Associative Memory Based on Double-Gating of Molecularly Linked Nanosystem Arrays: A Theoretical Scheme

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We discuss theoretically the properties of an associative memory (a system that can retrieve a stored pattern that is similar to the input pattern) based on the ideal conductive properties of a molecularly linked nanosystem array. Two schemes are considered for the memory based on the gate potential modulation of the drain-source current through the array. In the first scheme, the basic units of the electric circuit are nanosystems (e.g., nanoparticles) arranged in a series array. Each nanosystem is assumed to have two states of conductances, G_M and G_m ($G_M \gg G_m$), that can be tuned externally by the gate and backgate potentials. The bit sequence associated with a given pattern is stored as the components of a voltage vector. The input vector components are the gate voltages, and the stored vector components are the backgate voltages. The input pattern is compared with a given stored pattern by double-gating each nanosystem in the array with the respective components of the two vectors (the number of arrays is equal to the number of patterns to be stored). The individual conductances of the nanosystems in the array are high (G_M) when the input and stored vector components (bits) are equal and low (G_m) when they are different. The basis of the pattern recognition process is that the higher the number of bit coincidences, the higher the number of nanosystems in the array that are in states of high conductance and, therefore, the higher the drain-to-source current through the array. Alternatively, we consider also the properties of a second scheme in which the basic unit to be double-gated is the nanosystem array as a whole rather than a single nanosystem. Candidate experimental systems and simple circuit equations are considered for the two schemes that constitute preliminary steps toward future realizations of the associative memory using particular nanosystem arrays.

1. Introduction

The trend toward miniaturization of information storage and processing devices will eventually lead to nanoscale-based approaches. Combining the current complementary metal-oxide semiconductor (CMOS) technology with fundamentally new devices, such as single electron transistors (SETs), can bring out new functionalities, although designing hybrid circuits is difficult because of the different electrical characteristics.[1−3] Moreover, the performance of nanoscaled SETs can be affected by sample size distribution effects, randomly distributed background charges, co-tunneling effects, and thermal fluctuations at ambient conditions, making it difficult for transistor,[4] memory,[5] and circuit[2] operation. Simulation shows that networks of SETs showing high parallelism and redundancy are more robust against local fluctuations,[3] although well-defined structures in which the size and position of each building block (basic unit) are fixed at the nanoscale suffer from fabrication tolerance problems. An alternative route is based on less-ordered arrays, but these present electrical properties strongly dependent on the disorder characteristics.[6−9]

Metallic nanoparticles[10−13] positioned between two electrodes show transistor-like behavior and can be employed as the basic units of molecularly linked nanosystem arrays.[7−9,14−19] These arrays could be used in processing information devices, addressed electrically and, ideally, operated at temperatures close to ambient conditions. Although the experimental characterization and modeling of particular systems is currently receiving much attention, it is also necessary to design general electrical circuits that could perform information storage and -processing tasks using well-defined basic units. Binary logic gates based on the presence or absence of a single electron in nanosystems[2,20,21] and SET networks operating as character recognition circuits[2,3] have recently been proposed. Simple circuit equations showing fundamental properties together with detailed simulations of particular systems displaying the electrical characteristics required for the basic units of the circuit are necessary.

Associative memories are systems that can store patterns and retrieve them selectively by recognizing their similarity to an input pattern. We start here from the single-electron, stochastic, associative processing circuit by Yamanaka et al.[2] and propose an associative memory based on the ideal conductive properties of a molecularly linked nanosystem array. Two schemes are studied. In the first scheme, the basic unit of the electrical circuit is a nanosystem (e.g., a single nanoparticle or a group of a few nanoparticles) whose electrical conductance can be tuned externally by the gate potential. In this case, the drain-to-source current through each unit can be modulated by using a third (gate) voltage terminal,[14−16,22] and the conductance−gate potential curve is the electrical characteristic of the basic unit to be used in the circuit for the associative memory. The electrical circuit consists of an array of nanosystems arranged in series. Alternatively, we consider also the properties of a second scheme in which the basic unit to be gated is the nanosystem array (e.g., an array of many nanoparticles) as a whole. The electric circuit consists of a group of nanosystem arrays arranged now in parallel. Highly idealized circuit equations are obtained

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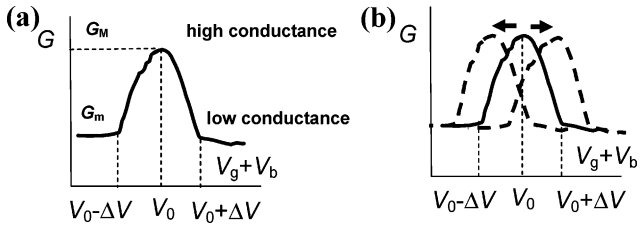

Figure 1. (a) The ideal conductance−gate potential curve characteristic of the basic unit to be used in the electrical circuits for the associative memory. The unit has only two states of conductances, $G_M \gg G_m$, that can be tuned by the sum of the gate and backgate potentials ($V_g + V_b$). (b) The shifts in the potential windows of the individual conductance curves are randomly distributed among the basic units and will give an effective conductance ratio G_M/G_m lower than the ideal one, as is shown schematically.

for the two schemes. Although the effects of the gate voltage on the conductance should ideally be studied using computer simulations that incorporate the characteristics of the individual nanosytems,[4,14] general circuit equations can constitute first-order, useful complements to system-dependent microscopic models.

Candidates to basic units of the associative memory must show significant gate potential modulation of the conductive properties (see Figure 1). Because the properties of metal nanoparticles have a strong sensitivity to applied potentials, nanoparticle arrays should be ideal candidates for memory elements. Experimental systems of interest could be multijunctions of SETs based on molecularly linked gold colloid particle chains,[22] self-assembled nanoparticle films,[23] and metallo-organic nanoscale networks[16] (a giant gate voltage effect producing a conductance variation of more than 100 times is reported in ref 16). In addition, ref 15 shows theoretically and experimentally that linear arrays of nanoparticles positioned between nanoelectrodes using DNA molecules have significant gate voltage effects on the drain-to-source current, which is just the property we propose to exploit here. Reference 24 shows theoretically that a linear array of metal ions, M-DNA, displays field-effect transistor (FET) properties: a gate voltage of 1 V at a distance of 5 nm is sufficient to decrease the conductivity of M-DNA by at least 10-fold. Other systems with different structures and conductive properties show also potentially useful characteristics. Self-assembled metalloprotein arrays act as FETs because of the gate potential effect on the redox resonance allowing significant current modulation, as shown theoretically and experimentally in refs 25 and 26. Single nanowires of conducting polymers polyaniline and polypyrrole show large gate-potential modulation in the electrical resistance of up to 3 orders of magnitude.[27] On the theoretical side, Monte Carlo simulations of the stochastic electron transport through a multiple-tunnel junction at low temperatures show that the calculated drain-to-source current[28] and the threshold potential for current to flow[4] can be modulated externally by the gate voltage. Certainly, the above list is not exhaustive, but it shows clearly that different nanosystems and arrays that exhibit transistor-like characteristics are currently available, although using them as the basic units of an electric circuit may be technically difficult.

Finally, for the associative memory concept, we employ the approach by Yamanaka et al.,[2] which is based on the double-gating of a single SET operating in parallel with other SETs. However, we will consider the ideal collective properties of the series arrangement constituted by the molecularly linked nanosystem array and use simple circuit concepts rather than detailed microscopic models for electron transport in a single SET.

2. An Ideal System and Two Schemes. Figure 1a shows schematically the ideal, approximately symmetrical conductance−gate potential curve characteristic of the basic unit. This unit could be a nanosystem (scheme 1) or a linear assembly (array) of nanosystems (scheme 2) gated as a whole. Using a phenomenological approach, we assume that this unit has only two states of conductances, G_M and G_m ($G_M \gg G_m$), that can be tuned by the gate potential (actually by the sum, $V_g + V_b$, of the gate and backgate potentials; see Figures 3 and 4). Admittedly, this constitutes a drastic simplification for the behavior of the basic unit, but this essential property is shown by the current−gate potential curve of a single SET[1] and, remarkably, by molecularly linked nanosystem arrays composed of a few nanoparticles.[15,22,28]

Although we assume typical, reasonably similar curves for every basic unit in the circuit, the fact is that finite size and shape distributions, background charges randomly distributed, and other deviations from the ideal behavior may shift the effective potential window of the individual curves. The shifts in the potential windows of the conductance curves should be randomly distributed among the basic units and will give an effective conductance ratio G_M/G_m lower than the ideal one, as shown schematically in Figure 1b.

We propose to use the characteristic conductance−gate potential curve of Figure 1 as the basis for the associative memory. Guimaraes et al.[3] have designed a Hamming neural network using SET devices, and Yamanaka et al.[2] have proposed an associative processing circuit robust to background-charge effects. Both networks were used to simulate pattern recognition tasks that are relevant to the problem considered here. In particular, we have considered in Figure 2 the pattern retrieval problem of ref 2. Each stored pattern consists of seven black and white segments that represent one of the 10 numbers 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. The black or white state of each segment corresponds, therefore, to a bit, and the above numbers can be

Figure 2. The stored patterns consist of seven black and white segments that represent a number (see Yamanaka et al.[2]). The black or white state of each segment corresponds to a bit, and the numbers are represented by $N = 10$ vectors, each one with $M = 7$ binary elements. The Hamming distance (HD) is the number of different bits between the input pattern (the number 5 within the square) and each of the 10 stored patterns.

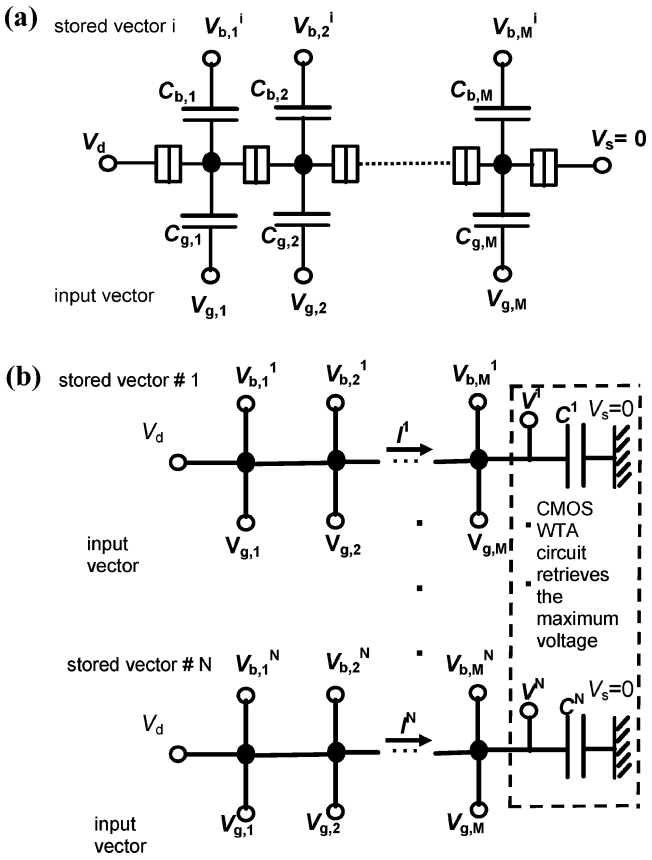

Figure 3. (a) Scheme of the multijunction array with $M = 7$ nanosystems (one per bit) arranged in series (scheme 1). The superscript i in the backgate voltage components makes reference to a given stored pattern ($i = 1, 2, ..., N$). The nanosystems (black circles) constitute the basic units of the circuit and are double-gated individually using the capacitors $C_{g,j}$ (gate) and $C_{b,j}$ (backgate), with $j = 1, 2, ..., M$. Insulating ligands (rectangles) link the nanosystem cores. Each of the $N = 10$ patterns (numbers) of Figure 2 can therefore be stored as a vector of $M = 7$ voltage components. V_d is the drain voltage, and $V_s = 0$ is the source voltage. (b) Electrical circuit to implement scheme 1. I^i is the electric current through the array i. The output capacitors of capacitance C^i act as the interfaces between the arrays and the CMOS winner-take-all (WTA) circuit[2,3] which selects that particular array k (pattern) whose capacitor voltage V^k reaches a prescribed voltage more rapidly.

represented by 10 vectors, each one with 7 binary elements.[2] The Hamming distance (HD) is the number of different bits between the input and a given stored pattern, as shown in Figure 2 for the case of pattern 5. We consider next the simplified circuits of Figures 3 and 4 for the associative memory to be used in the pattern retrieval problem of Figure 2.

Because patterns are digitalized in $M = 7$ bits and every basic unit is associated with a bit of information, an associative memory with a capacity to store $N = 10$ patterns is formed by $N \times M$ basic units. Figure 3a shows the proposed multijunction array with $M = 7$ basic units (one per bit) arranged in series (scheme 1). The units are nanosystems (black circles) double-gated individually using the capacitors $C_{g,j}$ (gate) and $C_{b,j}$ (backgate), with $j = 1, 2, ..., M$. Insulating ligands (rectangles) link the nanosystem cores. Each of the patterns i (numbers) of Figure 2 can be stored as a vector of seven components (voltages) as follows. Let us assume for simplicity that $V_0 = 0$ in Figure 1 and assign the voltages $+\Delta V/2$ to black segments and $-\Delta V/2$ to white segments. Therefore, the particular arrangement of black and white segments characteristic of a given number can be stored as the backgate voltage vector ($V_{b,1}^i$, $V_{b,2}^i$, ..., $V_{b,M}^i$). Let ($V_{in,1}$, $V_{in,2}$, ..., $V_{in,M}$) be the vector corresponding

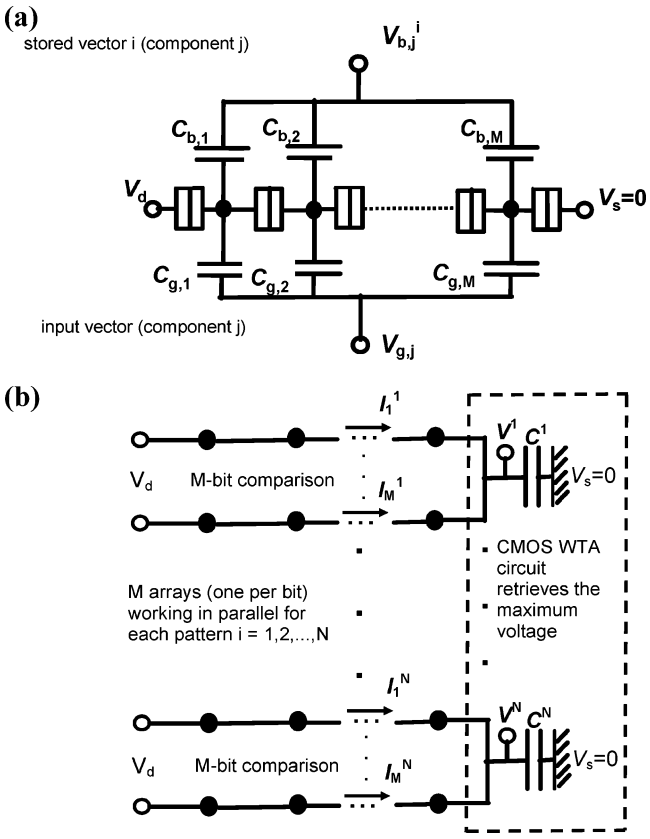

Figure 4. (a) Scheme of the multijunction array with the M nanosystems gated as a whole (scheme 2). The basic unit of the circuit is now the whole array with common gate and backgate voltages. In this case, the array corresponds to a given component, j, of the pattern i rather than to the whole pattern i of Figure 3a. (b) Electrical circuit to implement scheme 2. N circuits (one per pattern), each one composed by M arrays (one per bit) operating now in parallel, give a total number of $N \times M$ arrays. The gate and backgate potentials on each array are omitted for clarity. I_j^i is the electric current through the array j in the set of M parallel arrays corresponding to pattern i. The WTA circuit selects now that particular set k (pattern) of M parallel arrays whose voltage V^k reaches the prescribed voltage more rapidly.

to the input number to be compared with a given stored number. If we define the gate voltages of Figure 3a as the components of the complementary input vector, ($V_{g,1}$, $V_{g,2}$, ..., $V_{g,M}$) = $-$($V_{in,1}$, $V_{in,2}$, ...,$V_{in,M}$), the conductance of the basic unit j is

$$G_j^i(V_{g,j} + V_{b,j}^i) = \begin{cases} G_M \text{ if } (V_{g,j} + V_{b,j}^i) = 0 \rightarrow V_{in,j} = V_{b,j}^i \text{ (bit coincidence)} \\ G_m \text{ if } (V_{g,j} + V_{b,j}^i) = \pm\Delta V \rightarrow V_{in,j} \neq V_{b,j}^i \text{ (bit difference)} \end{cases} \quad (1)$$

where we have employed the curve of Figure 1a with $V_0 = 0$. Therefore, the individual conductances G_j^i of the basic units $j = 1, 2, ..., M$ are high (G_M) when the input and stored vector components (bits) are equal and low (G_m) when they are different. This forms the basis of the pattern recognition process, as we will see later.

To implement the associative memory, we need to compare the input number with every stored number and retrieve the most similar one (the pattern with the larger number of bit coincidences). This is shown in Figure 3b, where the superscript $i = 1, 2, ..., N$ in the backgate voltage components makes reference to the stored number. For every array in Figure 3b, V_d is the drain voltage and $V_s = 0$ is the source voltage. As is well-known,[2,3] output capacitors of relatively large capacitances

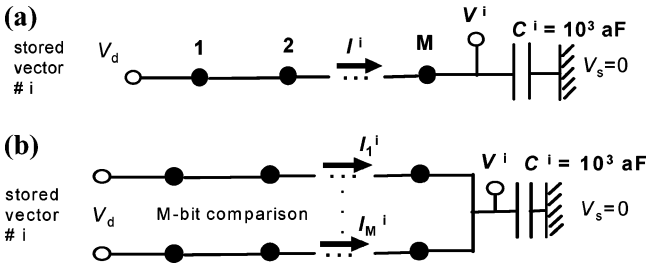

Figure 5. (a) Scheme 1: scheme of the circuit corresponding to pattern *i*. *M* basic units (nanosystems here) are double-gated individually (see Figure 3a) and arranged in series. (b) Scheme 2: scheme of the circuit corresponding to pattern *i*. *M* basic units (arrays composed of *M* nanosystems each) are double-gated as a whole (see Figure 4a) and arranged in parallel.

can be used as interfaces between SET and CMOS circuits. We will assume in Figure 3b that $C^i = 1$ fF $\gg 1$ aF ($i = 1, 2, ..., N$) because 1 aF is a typical value for the capacitance of a monolayer-protected metallic cluster.[29,30] The current I^i gives rise to the time-dependent potential, V^i, across the end capacitor, C^i, for each array $i = 1, 2, ..., N$ of Figure 3b. These potentials are the inputs to the CMOS winner-take-all (WTA circuit), which selects that particular array, *k*, whose capacitor voltage, V^k, reaches a prescribed voltage more rapidly.[2,3] This should correspond to the stored number with the lowest HD with respect to the input number (see Figure 2): the higher the number of bit coincidences between the input and the stored number, the higher the number of basic units in states of high conductance (see eq 1) and, therefore, the higher the capacitor charging current through the array (see Figure 3b).

As an alternative to the circuit of Figure 3, Figure 4a shows the multijunction array with *M* nanosystems gated as a whole (scheme 2). The basic unit of the circuit is now the whole array with common gate and backgate voltages. Figure 4b shows *N* circuits (one per pattern), each one composed by *M* arrays (one per bit) operating now in parallel. Note that scheme 2 needs a total number of *N* (patterns = numbers) × *M* (bits per pattern = vector components per number) arrays instead of the *N* arrays used in scheme 1 (compare Figure 4b with Figure 3b; although the number of nanosystems in each array is unspecified in scheme 2, we will assume *M* nanosystems per array, as in the case of scheme 1). The WTA circuit will select now that particular set *k* of *M* parallel arrays whose voltage V^k reaches the prescribed voltage more rapidly. Note that because the whole array is double-gated in Figure 4a, the conductances G_M and G_m refer now to the electrical states of the complete array (the basic unit of scheme 2) and not to the states of a single nanosystem (the basic unit of scheme 1) in the array. Because it could prove difficult to apply double gates on every nanosystem in the array, the circuit of Figure 4b can be easier to realize experimentally than that of Figure 3b. However, scheme 1 may still be technically feasible if we assume that the basic unit of Figure 3b is a nanosystem composed of a few nanoparticles (see, e.g., Figure 1 of ref 15) instead of only one nanoparticle.

We consider next the modeling of the circuits in Figures 3 and 4. Instead of using microscopic, system-dependent approaches for electron transport through every nanosystem, we propose simple phenomenological equations for the ideal electrical circuits of Figures 5a (scheme 1) and 5b (scheme 2). In the first case, *M* basic units are double-gated and arranged in series for each pattern $i = 1, 2, ..., N$. According to eq 1 and Figure 1, the inverse of the equivalent conductance of the series arrangement in Figure 5a is

$$\sum_{j=1}^{M} 1/G_j^i(V_{g,j} + V_{b,j}^i) = \mathrm{HD}^i/G_m + (M - \mathrm{HD}^i)/G_M \quad (2)$$

where G_j^i is the effective conductance of nanosystem *j* in array *i* and HD^i is the Hamming distance between the input pattern and the stored pattern *i*. Note that HD^i and $(M - \mathrm{HD}^i)$ are also the number of basic units in states of low and high conductances, respectively. Assuming a purely resistive behavior for the nanosystems in the array (the capacitive coupling of the basic units[4,31] and other nonideal effects are ignored), the charge, Q^i, of the capacitor C^i increases with time, *t*, as

$$\frac{dQ^i}{dt} = \left(V_d - \frac{Q^i}{C^i}\right)\frac{1}{\sum_{j=1}^{M} 1/G_j^i(V_{g,j} + V_{b,j}^i)} \quad (3)$$

Solving eq 3 for the charge with Q^i $(t = 0) = 0$ (all capacitors *i* are uncharged initially) and taking into account that the potential drop across the capacitor is $V^i(t) = Q^i(t)/C^i$ (see Figure 5a), we obtain

$$V^i(t)/V_d = \left\{1 - \exp\left[-\frac{1}{(\mathrm{HD}^i(G_M/G_m) + (M - \mathrm{HD}^i))}\frac{t}{(C^i/G_M)}\right]\right\} \quad (4)$$

Consider now the case of Figure 5b, in which *M* basic units (arrays of *M* nanosystems in series here) are double-gated and arranged in parallel for each pattern $i = 1, 2, ..., N$. Equation 1 is still formally valid, but G_j^i is now the effective conductance of array *j* in the set of *M* parallel arrays for pattern *i* (see Figure 4b). Applying a similar procedure for the circuit in Figure 5b, we obtain

$$\sum_{j=1}^{M} G_j^i(V_{g,j} + V_{b,j}^i) = \mathrm{HD}^i G_m + (M - \mathrm{HD}^i)G_M \quad (5)$$

for the effective equivalent conductance of the parallel arrangement. The charge, Q^i, of the capacitor C^i increases now with time as

$$\frac{dQ^i}{dt} = \left(V_d - \frac{Q^i}{C^i}\right)\sum_{j=1}^{M} G_j^i(V_{g,j} + V_{b,j}^i) \quad (6)$$

and the potential across capacitor *i* changes with time according to the equation

$$V^i(t)/V_d = \left\{1 - \exp\left[-(\mathrm{HD}^i(G_m/G_M) + (M - \mathrm{HD}^i))\frac{t}{(C^i/G_M)}\right]\right\} \quad (7)$$

Note that although large gate effects related to a redox state-mediated electron transport have been reported for single molecules,[32] the equivalent conductance laws of molecule arrangements are not trivial.[33] Therefore, eqs 2 and 5 constitute only first-order approximations for real nanoscaled circuits. Moreover, the results in eqs 4 and 7 are based on the ideal conductance curve of Figure 1 and the simplified equivalent circuit of eqs 3 and 6. Contrary to the above equations, the operation of nanoscaled SETs is not deterministic because

single-tunneling events occur randomly.[2] The Monte Carlo simulation and master equation methods for circuit analysis may be employed, but they are time-consuming,[1,4,5,28] especially for nanoscaled circuits with many basic units.[2,3] Moreover, established theoretical approaches for electronic tunneling through junctions of ideal SETs cannot be directly applied to disordered arrays, and corrections are usually needed in networks of nanoscale metallic islands separated by insulating ligands.[6−9] In these cases, charge transport is dominated not only by the single-electron charging energies and the tunnel resistances of the insulating ligands that separate the metallic cores but also by the structural disorder and the effective dimensionality of the current paths through the network.[6,9,31,34]

Therefore, for the sake of simplicity, we have assumed that the collective operation of many basic units in the array of scheme 1 can be described in terms of the individual conductances of the basic units, ignoring the system-dependent[4,5,15,18,19,22,24,26,35] coupling between the units in the chain. This assumption might be problematic for scheme 1 because the electrical behavior of a set of nanoparticles is collective in nature (see, e.g., ref 36). However, experiments[15] and simulations[28] conducted at subambient temperatures show that the gate voltage modulation (the key characteristic to be exploited here) is still preserved for a certain range of voltages if the basic unit contains a small number of nanoparticles instead of only one nanoparticle. For scheme 2, we have assumed simply that the whole array can be described as a simple two-state system with externally controlled conductances $G_M \gg G_m$. Remarkably, experiments[6,34] and stochastic simulations of electron transport through capacitatively coupled multiple-tunnel junctions[4,31,35] show that threshold potentials separating two regions of significantly different conductances are usual in the current−voltage curves. The simulation results suggest that the threshold potential can be modulated by the gate voltage,[4,35] which gives qualitative support to scheme 2 (see also Section 3, later). Note finally that the fluctuations and capacitative couplings neglected in our simplified model are explicitly taken into account in the above simulations.

We emphasize finally that although the concept of using a double gate on a single SET to implement an associative memory has been advanced by Yamanaka et al.,[2] who studied the effect of background charges on the pattern recognition problem of Figure 2 using a SET-based architecture, our approach shows three significant differences compared to ref 2: (i) The conductive properties of a set of molecularly linked *nanosystems arranged in series* (the arrays of schemes 1 and 2) are used rather than those of a *single SET-based parallel architecture* (see Figure 4 of ref 2). Note that the collective properties of a nanosystem array should be more robust against fluctuations than the individual characteristics of a single SET in the sense that associating bit data to the presence or absence of a single electron in an isolated island should be less reliable than considering the conductive properties of the whole array. In particular, although both ref 2 and scheme 2 use parallel arrangements, Figure 4b associates the bit data to a linear array containing many connected islands, whereas the unit circuit of ref 2 relies on the electrical properties of a single island. (ii) Particular nanosystems suitable for the realization of the associative memory are discussed, together with possible practical problems. (iii) Deterministic model equations based on simple circuits in which the basic unit has only two conductance states that can be tuned by the gate potential are proposed. As discussed above, this constitutes a rough approximation for experimental systems composed of many basic units, but it allows us to discuss general properties in terms of simple concepts that do not depend on the particular structural and transport details of the system considered.

3. Results and Discussion

Figures 6−8 present typical results obtained using schemes 1 and 2 for the patterns of Figure 2 and different values of the conductance ratio G_M/G_m. The input pattern is assumed to be the number 5 in Figure 2. Figure 6 shows the transient behavior of the capacitor potentials V^i normalized to V_d for the circuit of scheme 1 (see Figure 3b) in the cases $G_M/G_m = 2$ (a), 10 (b), and 100 (c), with $G_M = 10^{-7}\ \Omega^{-1}$. This conductance corresponds to a characteristic capacitor charging time, $C^i/G_M = 10$ ns, although the times in the curves of Figure 6 are much higher because the equivalent circuit conductance depends also on M, G_m, and HD^i (see eqs 2 and 5). Array currents and capacitor charges are on the order of $I^i \sim 1$ nA and $Q^i \sim 10e$ for $V_d = 1$ mV, respectively, where e is the fundamental charge.

The parameters introduced in the calculations are characteristic of nanosystems. Output capacitors of relatively large capacitances, $C^i = 1$ fF $\gg 1$ aF, can be used as interfaces between SET and CMOS circuits (see refs 2 and 3). Note that 1 aF is the typical nanoparticle capacitance for a monolayer-protected metallic cluster.[11−13,29] The nanowire resistances for the conducting polymers of ref 27 are in the range $10^6-10^8\ \Omega$, giving a mean conductance $G = 10^{-7}\ \Omega^{-1}$. In addition, conductance ratios $G_M/G_m > 10$ are reported in the M-DNA simulations of ref 24. Finally, typical currents for the multijunctions of ref 28 are 1−10 nA for drain-to-source voltages in the range 1−5 mV.

The maximum potentials attained for each array $i = 1, 2, ..., N$ at sufficiently long times could be compared to a prescribed potential lower than V_d. The capacitor that reaches this prescribed potential at a shorter time corresponds to the pattern i most similar to the input pattern (the number 5 in Figures 6 and 7).[2] As expected, the maximum potentials of Figure 6 decrease with increasing the Hamming distance for the patterns of Figure 2. Note that disordered patterns similar but not exactly equal to any of the stored patterns may also be used as input patterns by introducing the appropriate values of HD^i in eqs 4 and 7 for each pair of input and stored patterns. The circuits of Figures 3b and 4b would then retrieve the stored pattern most similar to the disordered input pattern in this case.

The comparison of Figure 6b with 6c shows clearly the need to use nanosystems with high conductance ratios, G_M/G_m, for the optimal associative memory operation. The comparison of Figure 6b with 6a shows also that if the effective value of G_M/G_m is significantly lower than the ideal one (see Figure 1a) because of the different conductance−gate potential curves of the basic units (see Figure 1b), the scheme will be of limited validity. This should be a point of especial concern here, since most nanosystems tend to show relatively wide size and shape distributions that may lead to operational problems. Clearly, ideal systems should show both low variances in the characteristics of the basic units (the nanoparticle potential window to be used in the gating must be reasonably uniform) and high ratios G_M/G_m.

Figure 7 shows the transient behavior of the dimensionless potentials V^i/V_d for the circuit of scheme 2 in Figure 4b and the cases $G_M/G_m = 2$ (a), 10 (b), and 100 (c), with the same conditions as Figure 6. In this case, increasing G_M/G_m from the reference value of 10 does not improve significantly the pattern recognition (compare Figure 7b with 7c). As could be expected, decreasing G_M/G_m renders the associative memory useless

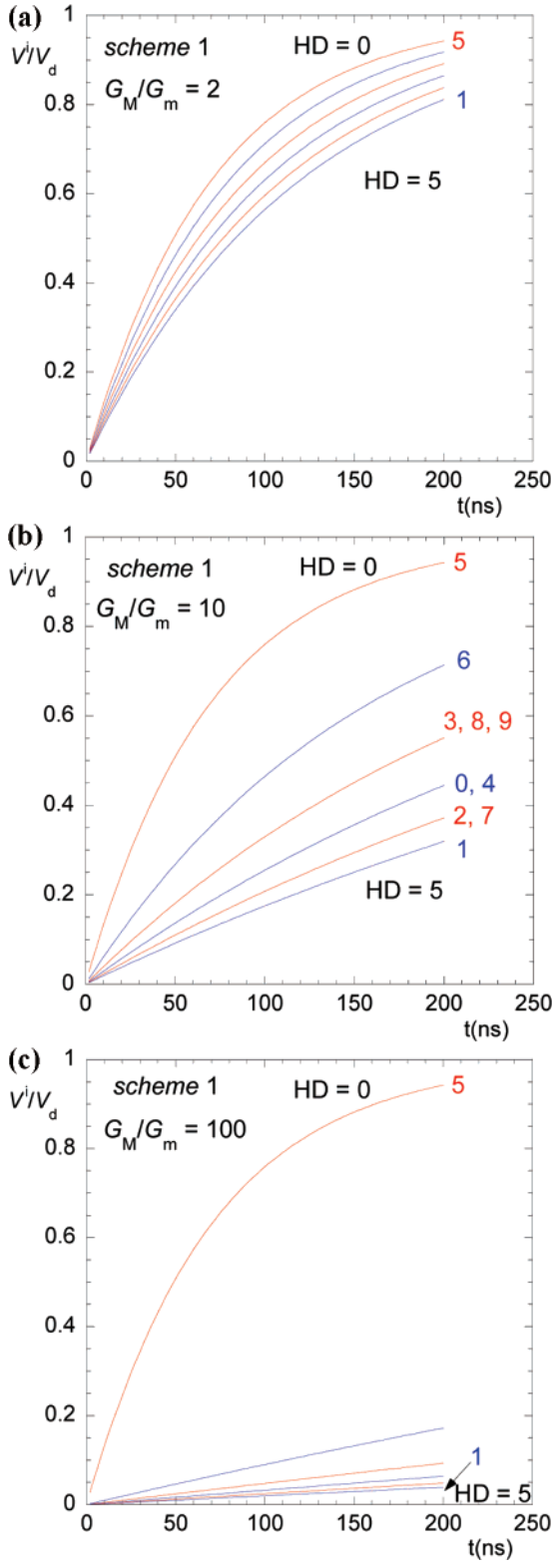

Figure 6. The transient behavior of V^i/V_d for the circuit of scheme 1 (see Figure 3b) in the cases $G_M/G_m = 2$ (a), 10 (b), and 100 (c), with $G_M = 10^{-7}$ Ω^{-1}. The maximum potentials attained for each array $i = 1, 2, ..., N$ at sufficiently long times can be compared to a prescribed potential to retrieve that pattern, i, that is equal to the input pattern (the number 5 here). The numbers in the curves correspond to the patterns of Figure 2.

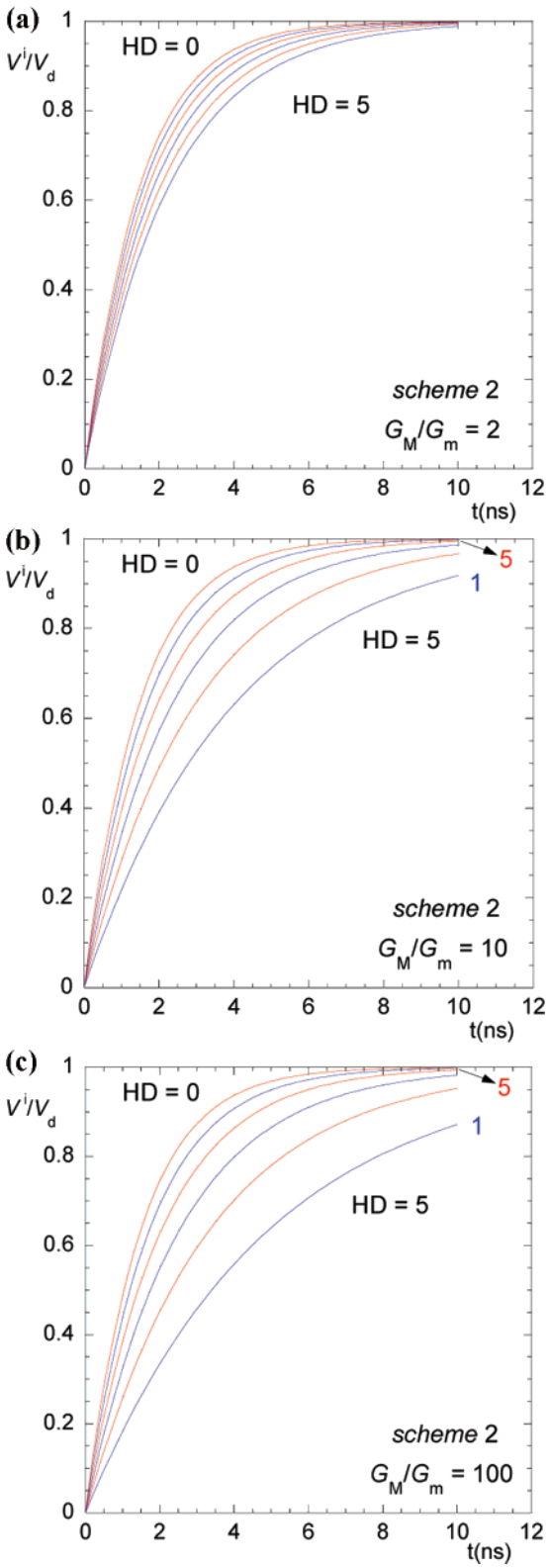

Figure 7. The transient behavior of potentials V^i/V_d for the circuit of scheme 2 (see Figure 4b) in the cases $G_M/G_m = 2$ (a), 10 (b), and 100 (c), with the same conditions as Figure 6.

(compare Figure 7b with 7a). Obviously, these properties, together with the shorter response times of Figure 7 as compared to those of Figure 6, are direct consequences of the parallel architecture used in scheme 2 (see Figure 4b), as opposed to the series architecture employed in scheme 1 (see Figure 3b). However, it may prove difficult to gate individually the nanoscaled basic units of scheme 1 while this gating is less stringent for the whole arrays of scheme 2. Therefore, if the circuit of Figure 4b is to be implemented because of its improved technical feasibility with respect to the circuit of Figure 3b, an additional nonlinear element should be added at the end of each

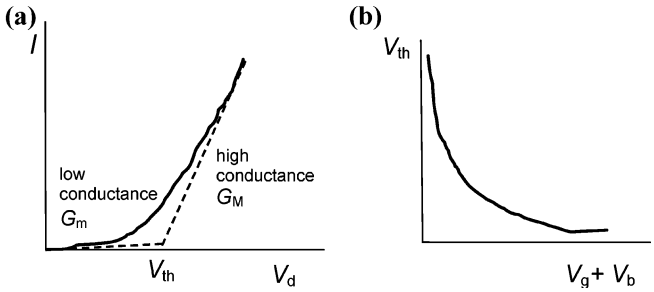

Figure 8. (a) The typical current (I)−voltage (V_d) curve of a nanosystem array shows a threshold voltage, V_{th}, that separates two regions of well-defined conductances, with $G_M \gg G_m$. (b) The threshold voltage, V_{th}, characteristic of the array could be used as the tunable property provided that V_{th} changes significantly with the sum of the gate and backgate potentials, ($V_g + V_b$), as shown schematically.

array to enhance discrimination between the respective currents. Alternatively, mesoscopic arrays formed by a metallic grain linked to two electrodes by organic ligands could be used as the basic units of the associative memory.[37] Because this system shows resonant behavior when the frequency of the applied voltage is close to the characteristic frequency of the oscillating grain,[38] a parallel arrangement of arrays with different natural frequencies can be excited selectively by an external electrical signal with the appropriate resonant frequencies. The highly nonlinear system response[38] should make possible efficient pattern retrieval also for the case of scheme 2. Finally, other bit maps with increased Hamming distances could be used to enhance discrimination between patterns.[3]

We consider now a possible practical realization for scheme 2. It has been shown experimentally that the drain-to-source current through a nanosystem array is close to zero for $V_d < V_{th}$ and follows a power law with V_d for $V_d > V_{th}$[6,34] (see Figure 8a here and Figure 2 of ref 6). Because the threshold potential V_{th} separates two regions of well-defined conductances $G_M \gg G_m$ (see Figure 8a), the potential V_{th} could be used as the electrical property of the basic unit (the array in scheme 2) instead of the conductance of Figure 1. Theoretical simulations for ideal linear arrays at low temperatures predict, indeed, that V_{th} can be tuned by the gate potential[4,28,35] (see Figure 8b here and Figure 5 of ref 4; note that the capacitive coupling of the nanosystems is not ignored in the computer simulations of ref 4). The rapid decrease of V_{th} with the gate potential, followed by a region of weaker dependence, makes the array potentially useful as an electrical switch, although background charges can reduce significantly the gate modulation.[4] In addition, because $G_M \gg G_m$ in this case, only the requirement of similar values of V_{th} for reasonably uniform arrays would now be necessary. The electrical circuit needed to exploit the threshold potential of the array in the associative memory may be similar to that of Figure 4. Gate and backgate voltages should now be applied to give $V_d < V_{th}(V_g + V_b)$ for bit difference (corresponding to low conductance G_m in Figure 8a) and $V_d > V_{th}(V_g + V_b)$ for bit coincidence (corresponding to high-conductance G_M in Figure 8a).

We may also compare the capacitor potentials, V^i, among themselves instead of comparing them with a prescribed potential. Figure 9 considers the normalized voltages V^i_{max}/V_T obtained with the electrical circuit of scheme 1 for the different patterns of Figure 2, where V^i_{max} is the maximum potential attained by the capacitor in array i at the longer times considered in Figure 6 and V_T is the sum of the maximum potentials for all arrays $i = 1, 2, ..., N$. Therefore, the normalized potentials of Figure 9 correspond roughly to the probabilities of retrieving

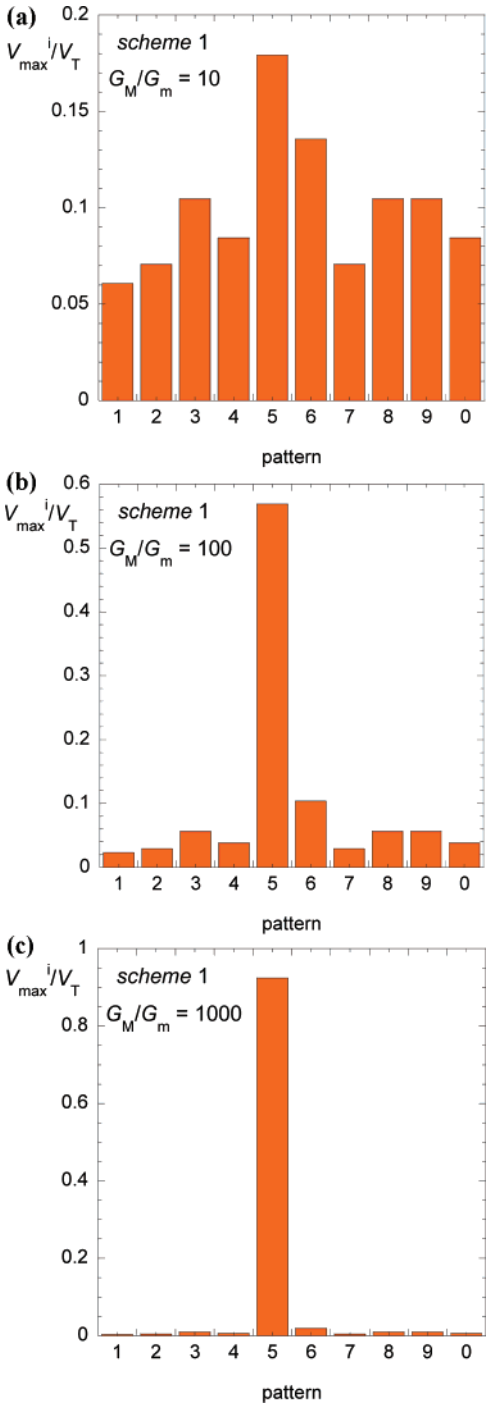

Figure 9. The normalized voltages V^i_{max}/V_T obtained with the electrical circuit of scheme 1 for the different patterns of Figure 2 in the cases $G_M/G_m = 10$ (a), 100 (b), and 1000 (c), with the same conditions as Figure 6. V^i_{max} is the maximum potential attained by the capacitor in array i at the longer times considered in Figure 6, and V_T is the sum of these maximum potentials for all arrays $i = 1, 2, ..., N$.

the respective stored patterns (numbers) when the input pattern is the number 5 of Figure 2. As expected, the lower the Hamming distance between the input pattern and a given stored pattern, the higher the probability of retrieving this stored pattern (see Figures 2 and 9). Figure 9 shows also the essential role of the conductance ratio G_M/G_m in the associative memory. Clearly, increasing the number of bits associated with each pattern[3] could allow better retrieving properties.

In summary, although the inherent uncertainties associated with the fabrication and operation of nanosystem arrays are

likely to produce significant experimental deviations from the predictions of Figures 6, 7, and 9, the ideal conductive properties of a double-gated molecularly linked nanosystem array are of conceptual interest. Scheme 1 shows better discrimination properties than scheme 2, and it could be considered experimentally if the basic unit in the series arrangement of Figure 3b is constituted by a few nanoparticles (perhaps inserted on DNA molecules as building blocks[15,24]) with common gate and backgate voltages instead of only one nanoparticle. Even for this case, however, the conditions on positioning and uniformity of nanoparticles and electrodes are very demanding for scheme 1 because significant gate control could be achieved only when the electrode is sufficiently close to the nanosystem[15,22,24,39,40] (a gate voltage of 1 V at a distance of 5 nm is predicted to decrease the conductivity of M-DNA by at least 10-fold;[24] see also the quantum transport simulations of ref 40, where gate-induced switching between states of significantly different conductances are predicted for a polythiophene molecule attached to ideal metal contacts). Note also that the close proximity of neighboring gate electrodes might also induce undesirable electrostatic couplings in the case of scheme 1. Hopefully, a certain degree of disorder could still be allowed in practical applications, provided that the gate effects on the basic units of the array are important. Moreover, because we propose to exploit some collective (e.g., electromechanical[16,24]) effect of the gate voltage on the conductance of the nanosystem array rather than the microscopic properties of a single, nanoscaled-SET,[2] the scheme could be operative at not extremely low temperatures. Finally, if monolayer-protected clusters (MPC)[10−12,29] with metallic cores were to be used as the basic units of the circuit, the coupling of electrical oscillations to mechanical vibrations could be achieved by bridging the MPC to the electrode. Indeed, the soft dielectric chains surrounding the core could lead to time-dependent tunneling lengths, $x(t)$,[37] and a rich electrodynamics because of the exponential dependence of the tunnel resistance on $x(t)$. In particular, the use of a time-dependent bias voltage[38] could make possible an oscillatory (frequency-based) associative memory scheme. Further work along this line is in progress.

4. Conclusions

We have explored the properties of an associative memory (a system that can retrieve a stored pattern that is similar to the input pattern) on the basis of the ideal conductive properties of a molecularly linked nanosystem array. Two schemes that are based on the gate potential modulation of the drain-source current through the array are considered. In the first scheme, the basic units of the electrical circuit are nanosystems arranged in series. Each nanosystem has only two states of conductances, G_M and G_m ($G_M \gg G_m$), that can be tuned externally by the gate and backgate potentials. The bit sequence that defines a given pattern is stored as the components of a voltage vector. The input vector components are the gate voltages and the stored vector components are the backgate voltages. The input pattern is compared with a given stored pattern by double-gating each nanosystem in the array with the respective components of the two vectors. The individual conductances of the nanosystems in the array are high (G_M) when the input and stored vector components (bits) are equal and low (G_m) when they are different. The basis of the pattern recognition process is that a high number of bit coincidences corresponds to a high number of nanosystems in states of maximum conductance (and therefore to a high drain-to-source current through the array). Alternatively, we consider the properties of a second scheme in which the nanosystem array as a whole is the basic unit to be double-gated. Experimental systems that show the properties required for the basic units, together with some practical problems that should be addressed, are also mentioned. Admittedly, the model equations are highly idealized and ignore effects such as nondeterministic circuit operation, background charges randomly distributed, specific couplings between adjacent units, etc. However, some preliminary steps toward future realizations of the associative memory using particular molecularly linked nanosystem arrays have been given.

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