

8

Converters

Frequency Down Converter

In many situations for radio frequency receivers, there is a need for shifting a high frequency input waveform into a low frequency waveform. The operation is called down conversion. In frequency domain, it consists in shifting a high frequency information contained in frequency f_{in} to a lower frequency f_{out} , as illustrated in figure 8-1.

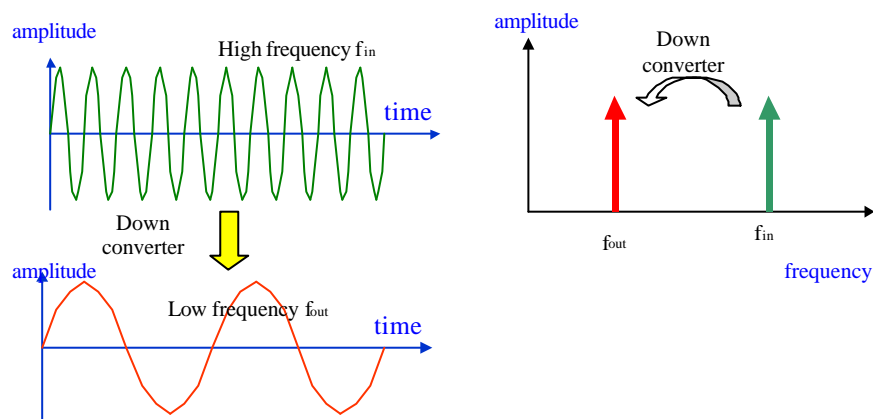


Fig. 8-1. Principles for down conversion

One very simple solution consists in using a transmission gate with a very accurate tuning of the gate clock. As an illustration, we use a 1.900 GHz sinusoidal wave, and a 1.818 GHz sampling signal (550 ps period). The expected output frequency is therefore $1.900 - 1.818 = 0.082$ GHz, that is 82MHz. The layout of the sample circuit is a simple transmission gate with an RC filter (Figure 8-2).

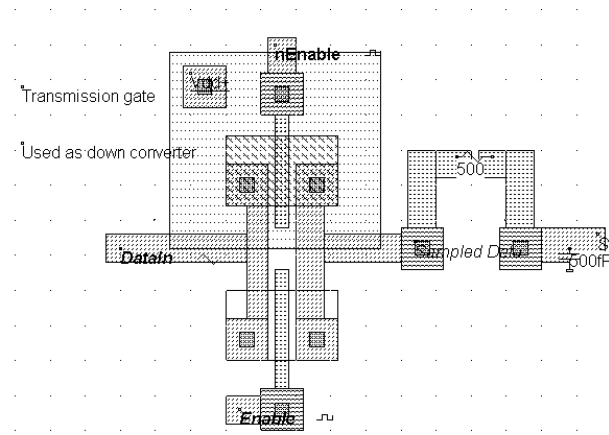


Fig. 8-2. Layout of the transmission gate and RC filter used for down conversion (DownConverter.MSK)

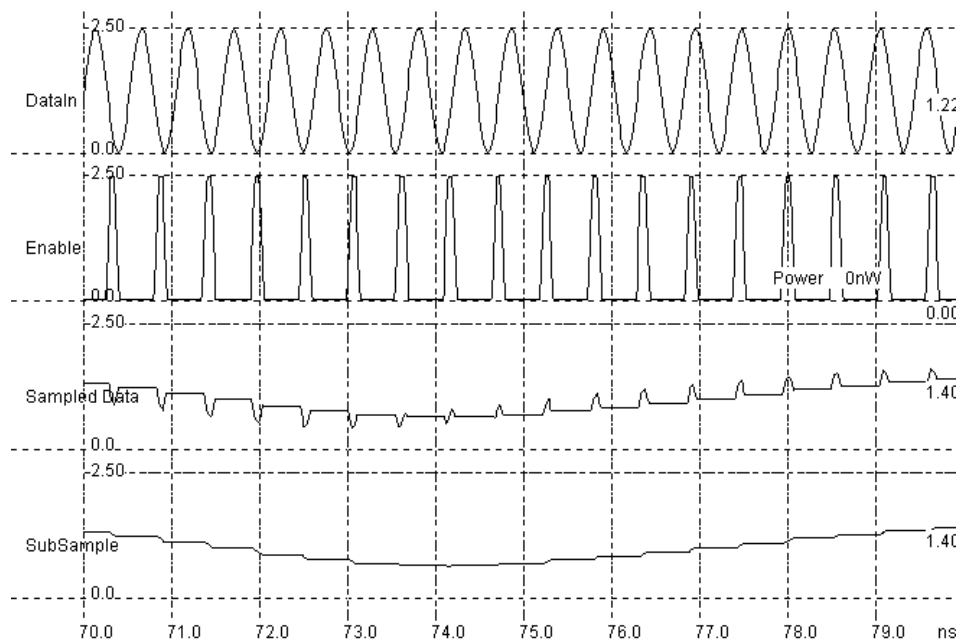


Fig. 8-3. Down conversion of the 1.9GHz input sinusoidal wave to a low frequency

The sampling at a frequency slightly slower than the input frequency leads to a signal at low frequency at the output of the transmission gate. (Figure 8-3). With a simple RC filtering, the output signal becomes a sinusoidal wave with a frequency equal to the difference of the initial waveform and the gate control frequency. When simulating at a large time scale (Figure 8-4), and asking for the evaluation of the frequency of the resulting waveform, we find 83MHz, very close from the expected 82MHz resulting from the subtraction 1900 MHz-1818MHz.

In figure 8-4, the effect of filtering is clearly seen. The spikes have disappeared, and a clean sinusoidal waveform remains.

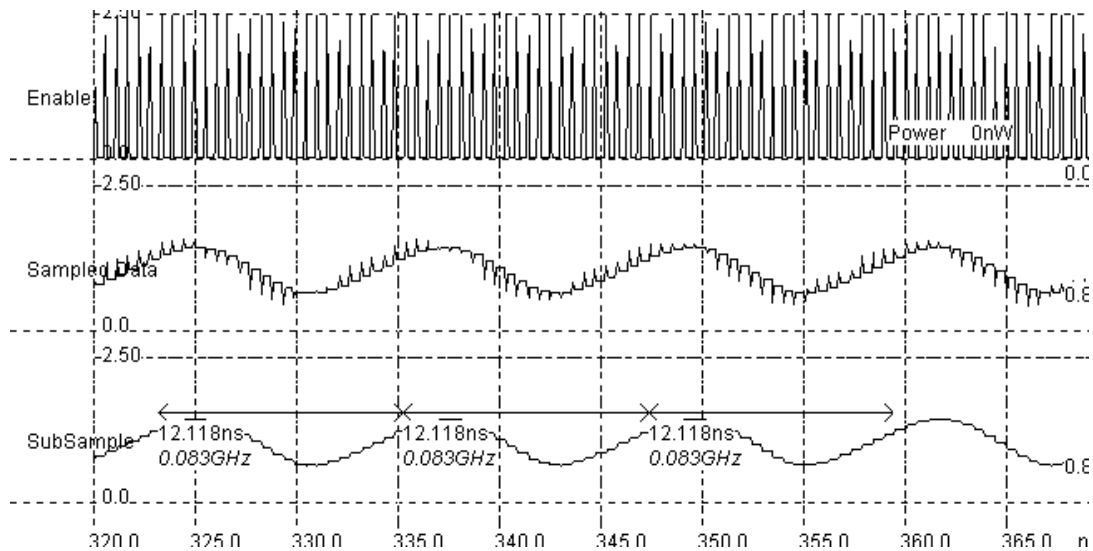


Fig. 8-4. Down conversion of the 1.9GHz input sinusoidal wave to 83MHz

Analog-Digital Converter

The analog-digital converter converts an analog value **V_{in}** into a two-bit digital value called A0,A1. The flash converter uses three converters and a coding logic to produce A0 and A1 (Figure 8-1). A very complex logic circuit and 255 comparators would be used for an ADC eight-bit flash.

The polysilicon has a high resistance (50 per square) and can be used as a resistor network (Left of Figure 8-2), which generates intermediate voltage references used by the voltage comparators located in the middle. The resistance symbol is inserted in the layout to indicate to the simulator that an equivalent resistance must be taken into account for the analog simulation.

Analog Input V _{in}	C0	C1	C2	A1	A0
V _{in} <1.25V	0	0	0	0	0
1.25<V _{in} <2.5V	1	0	0	0	1
2.5<V _{in} <3.75V	1	1	0	1	0
V _{in} >3.75	1	1	1	1	1

Open-loop amplifiers are used as voltage comparators. The comparisons address the decoding logic situated to the right and that provides correct A0 and A1 coding.

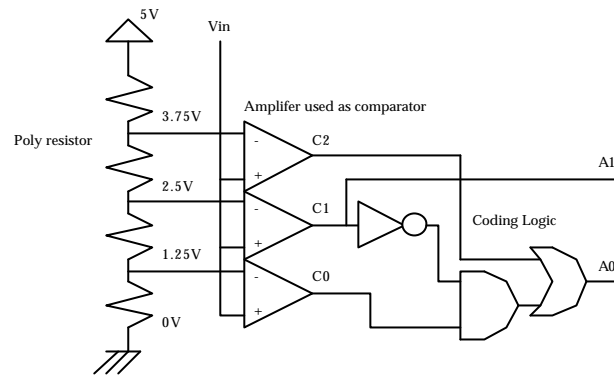


Fig. 8-1. Node description and schematic diagram of the analog-digital converter (ADC.MSK).

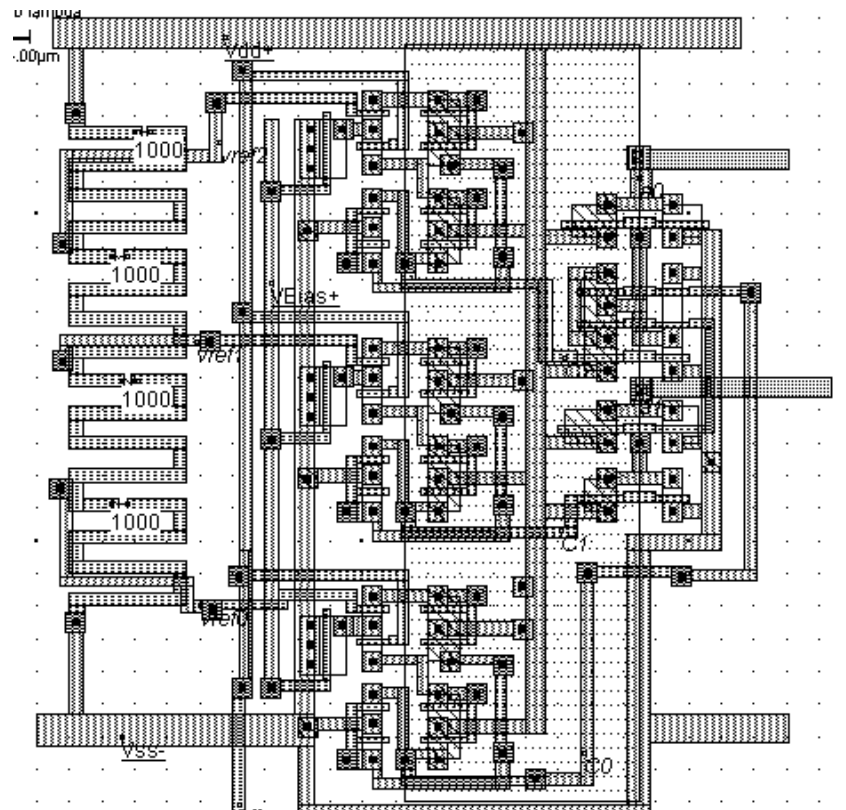


Fig. 8-2. Design of the analog-digital converter (ADC.MSK).

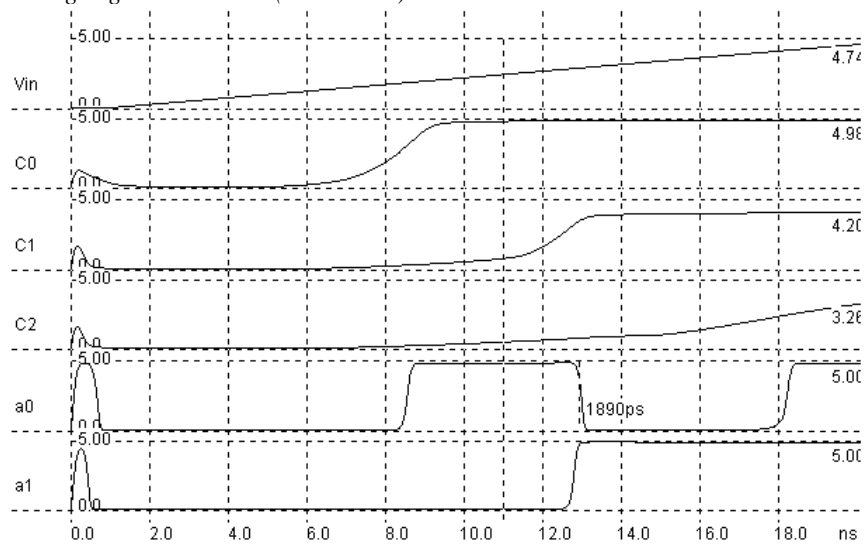


Fig. 8-3. Simulation of the analog-digital converter (ADC.MSK).

In the simulation shown in Figure 8-3, the comparators C0 and C1 work well but the comparator C2 is used in the upper limit of the voltage input range. The generation of combinations 00,01 and 10 is correct. The generation of 11 is slow.

Digital-Analog Converter

The digital-analog converter converts a digital three-bit input (A0,A1,A2) into an analog value **Vout**. The polysilicon resistive net gives intermediate voltage references which flow to the output via a transmission gate net. The resistance symbol is inserted in the layout to indicate to the simulator that an equivalent resistance must be taken into account for the analog simulation. The schematic diagram and layout of the digital-analog converter are shown in Figure 8-4.

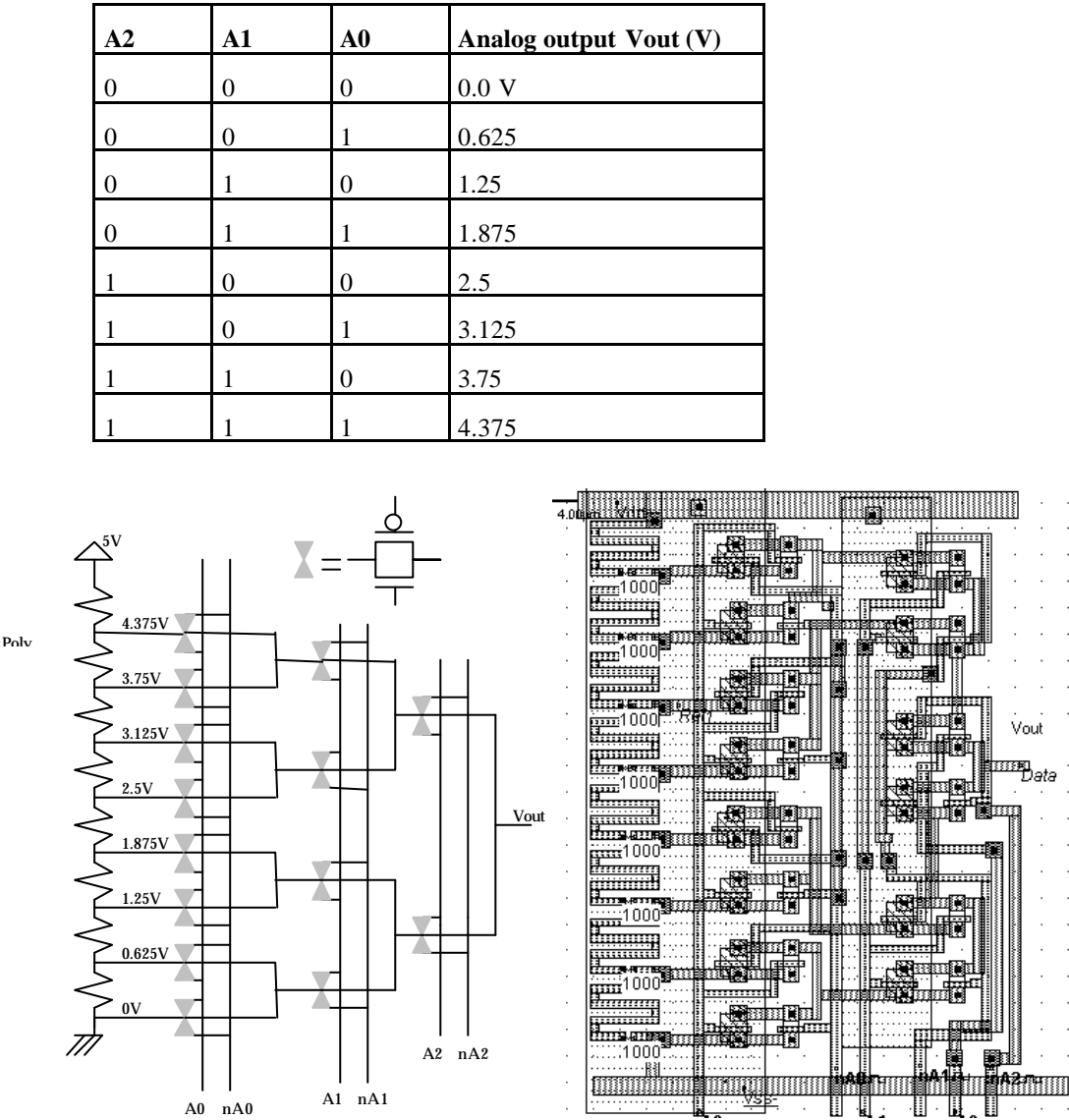


Fig. 8-4. Schematic diagram and implementation of the digital-analog converter (DAC.MSK).

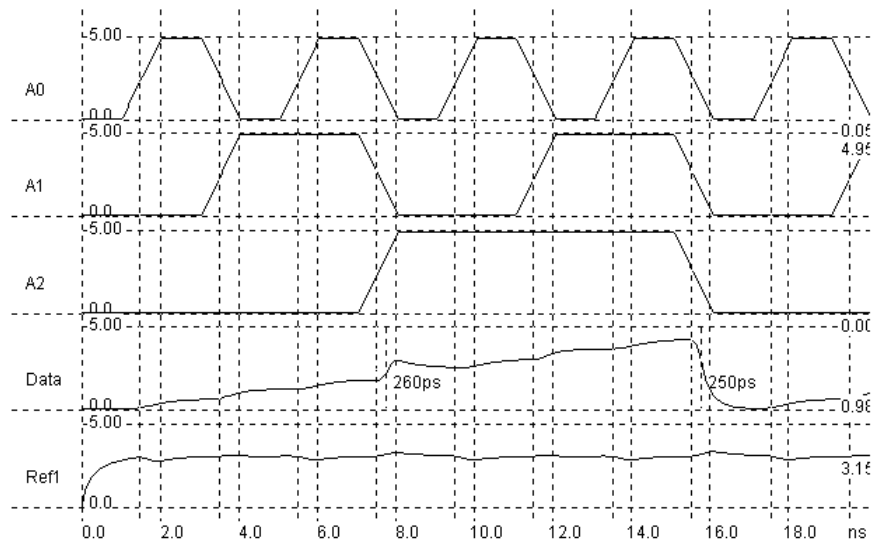


Fig. 8-5. Simulation of the digital-analog converter (DAC.MSK).

The simulation of the DAC (Fig. 8-5) shows a regular increase of the output voltage **Vout** with the input combinations, from 000 (0V) to 111 (4.375V). Each input change provokes a capacitance network charge and discharge.

Sample and Hold circuit

During the conversion from analog to digital, the input signal must be kept constant. This operation is called sample-and-hold. The transmission gate can be used as a sample and hold circuit. The layout of the transmission gate is reported below.

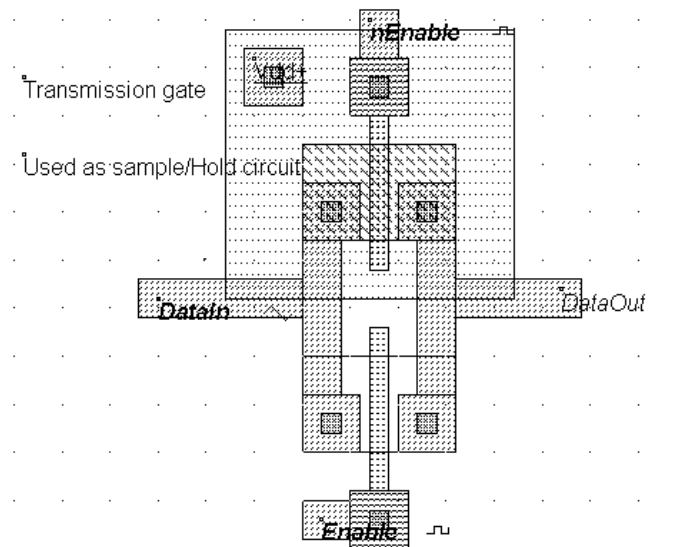


Fig. 8-6. The transmission gate used to sample analog signals (SampleHold.MSK)

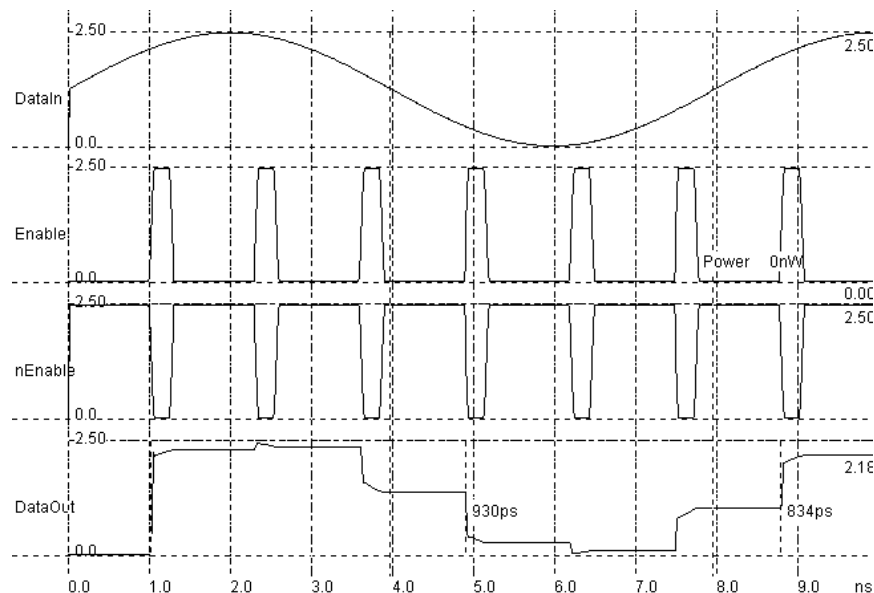


Fig. 8-7. Effect of sampling

The effect of sample and hold is illustrated in figure 8-7. When sampling, the transmission gate is turned on so that the sampled data DataOut reaches the value of the sinusoidal wave DataIn. The sampling effect appears more clearly in figure 8-8, in which the voltage curves have been superimposed. When the gate is off, the value of the sampled data remains constant. This is mainly due to the parasitic capacitance of the node, which has a value of 1.9 fF, as extracted in a CMOS 0.25 μ m process.

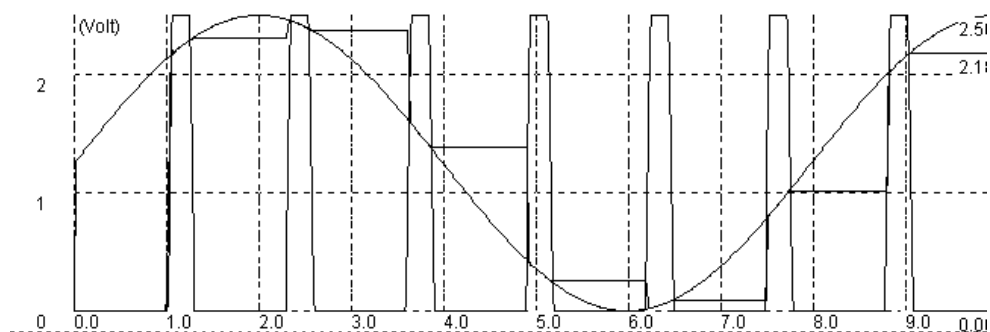


Fig. 8-8. Effect of sampling on a sinusoidal wave (SampleHold.MSK)

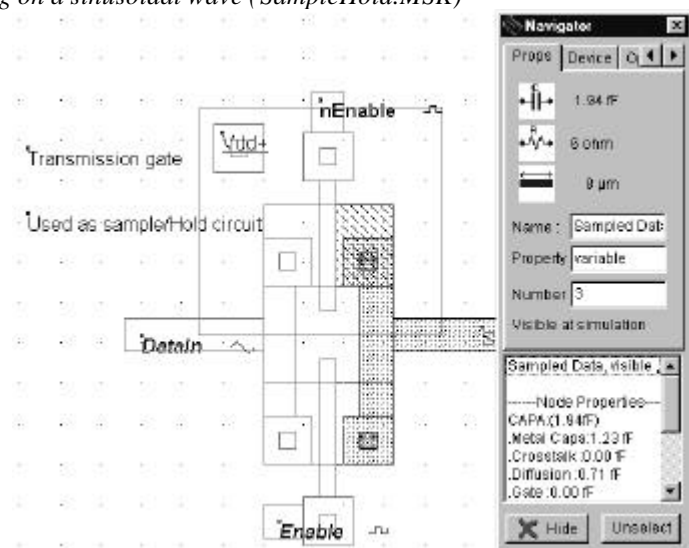


Fig. 8-9. The hold effect is related to the parasitic capacitance of the node "SampledData"

