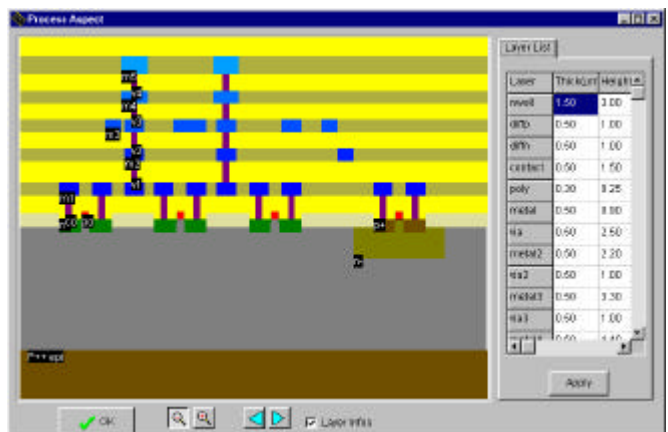
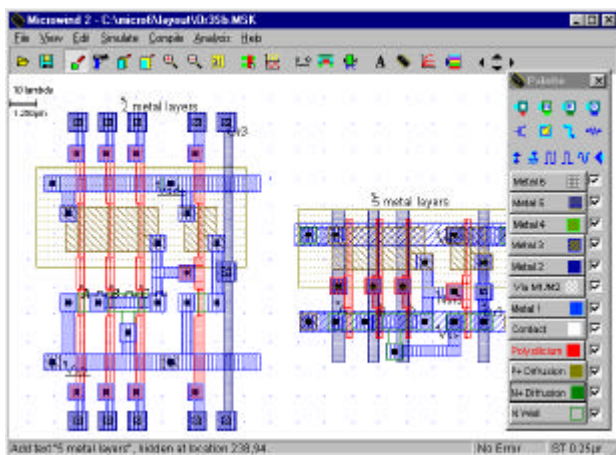
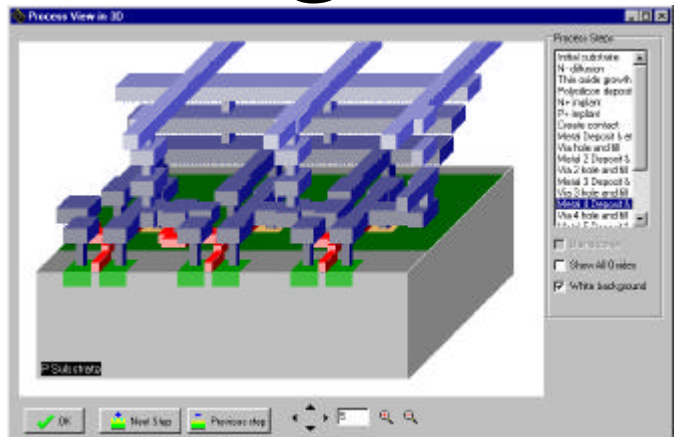
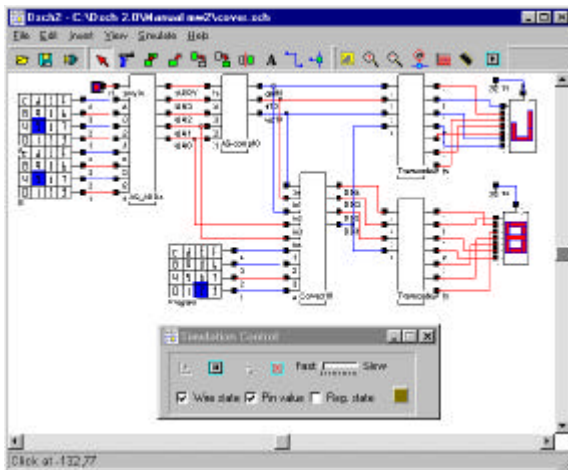


Introduction to deep-submicron CMOS circuit design



Etienne Sicard

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Glossary

<i>Back-End</i>	Interconnect fabrication steps.
<i>CMOS</i>	<i>Complementary - Metal - Oxide - Semi-conductor</i> . Basic name for the technology used to fabricate N-channel and P-channel MOS transistors.
<i>Deep submicron technology</i>	Lithography lower than 0.5 μm , including the 0.35 μm process (1996), 0.25 μm (1998) and 0.18 μm (1999).
<i>Front-End</i>	MOS device fabrication steps.
<i>MOS</i>	Abbreviation for Metal - Oxide - Semiconductor, representing the elementary transistor. The MOS exists in two versions: one with N channel, one with P channel. The early “metal” gate has been replaced by polysilicon.
<i>Level 1</i>	Logic level considered as “1”. In CMOS design, a logic level 1 is a voltage significantly higher than $V_{DD}/2$.
<i>Level 0</i>	Logic level considered as “0”. In CMOS design, a logic level 0 is a voltage significantly lower than $V_{DD}/2$.
<i>Lithography</i>	The smallest fabricated pattern. This dimension is roughly the distance between the drain and source of the transistor. It is also call the «technology ». For example, the Pentium III® is fabricated in 0.18 μm technology, that is a lithography of around 0.18 μm .
<i>SOI</i>	Silicon on Insulator. Very promising technological enhancement, featuring important speed improvement and compact cell layout.
<i>Ultra Deep submicron technology</i>	Lithography lower than 0.18 μm , including the 0.12 μm process (2000), 0.10 μm (2002) and 0.07 μm (2004).
<i>VDD</i>	Power supply. Never stops decreasing with technology. VDD is 2.5V in 0.25 μm technology.

MULTIPLIERS

<i>Value</i>	<i>Name</i>	<i>Standard Notation</i>
10^{18}	PETA	P
10^{15}	EXA	E
10^{12}	TERA	T
10^9	GIGA	G
10^6	MEGA	M
10^3	KILO	K
10^0	-	-
10^{-3}	MILLI	m
10^{-6}	MICRO	u
10^{-9}	NANO	n
10^{-12}	PICO	p
10^{-15}	FEMTO	f
10^{-18}	ATTO	a
10^{-21}	ZEPTO	z

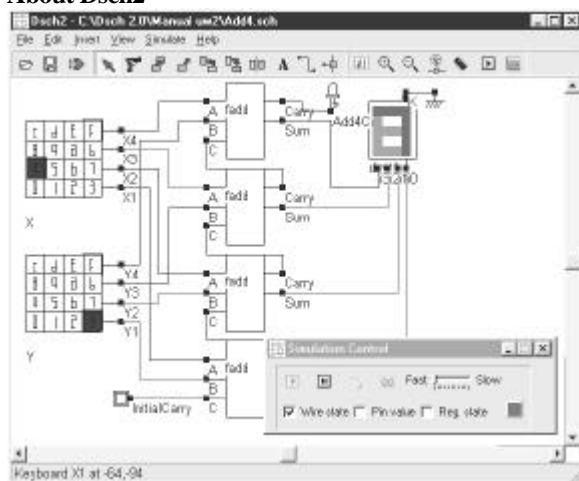
PHYSICAL CONSTANTS & PARAMETERS

<i>Name</i>	<i>Value</i>	<i>Description</i>
ϵ_0	$8.85 \text{ e}^{-14} \text{ Farad/cm}$	Vacuum dielectric constant
$\epsilon_r \text{ SiO}_2$	3.9 - 4.2	Relative dielectric constant of SiO_2
$\epsilon_r \text{ Si}$	11.8	Relative dielectric constant of silicon
$\epsilon_r \text{ ceramic}$	12	Relative dielectric constant of ceramic
k	$1.381 \text{ e}^{-23} \text{ J/}^\circ\text{K}$	Boltzmann's constant
q	$1.6 \text{ e}^{-19} \text{ Coulomb}$	Electron charge
μ_n	600 V.cm^{-2}	Mobility of electrons in silicon
μ_p	270 V.cm^{-2}	Mobility of holes in silicon
γ_{al}	$36.5 \cdot 10^6 \text{ S/m}$	Aluminum conductivity
ρ_{al}	$0.0277 \Omega.\mu\text{m}$	Aluminum resistivity
γ_{cu}	$58 \cdot 10^6 \text{ S/m}$	Copper conductivity
ρ_{cu}	$0.0172 \Omega.\mu\text{m}$	Copper resistivity
$\rho_{\text{tungstène (W)}}$	$0.0530 \Omega.\mu\text{m}$	Tungsten resistivity
$\rho_{\text{or (Ag)}}$	$0.0220 \Omega.\mu\text{m}$	Gold resistivity
μ_0	$1.257 \text{ e}^{-6} \text{ H/m}$	Vacuum permeability
T	$300^\circ\text{K} (27^\circ\text{C})$	Operating temperature

1 Introduction

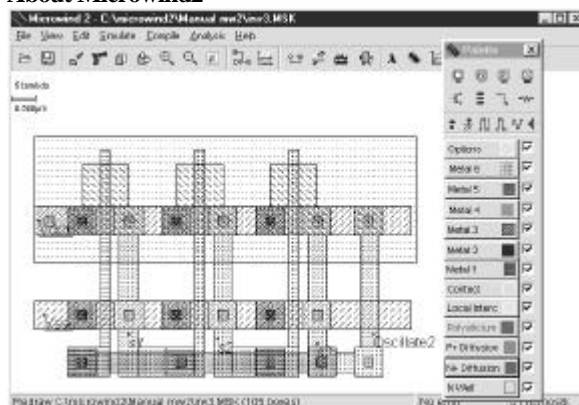
The present book introduces the design and simulation of CMOS integrated circuits, in an attractive way thanks to user-friendly PC tools Dsch2 and Microwind2.

About Dsch2



The DSCH2 program is a logic editor and simulator. DSCH2 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH2 provides a user-friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. A key innovative feature is the possibility to estimate the power consumption of the circuit. Some techniques for low power design are described in the manual.

About Microwind2



The MICROWIND2 program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to *Circuit Simulation* by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

The chapters of this manual have been summarized below. Chapter One describes the technology scale down and the major improvements given by deep sub-micron technologies. Chapter Two is dedicated to the presentation of the single MOS device, with details on the device modeling, simulation at logic and layout levels. Chapter Three presents the CMOS Inverter, the 2D and 3D views, the comparative design in micron and deep-submicron technologies. Chapter Four concerns the basic logic gates (AND, OR, XOR, complex gates), Chapter Five the arithmetic functions (Adder, comparator, multiplier, ALU) and describes a student project concerning a 4-bit binary to Decimal adder. The latches and memories are detailed in Chapter Six.

As for Chapter seven, analog cells are presented, including voltage references, current mirrors, operational amplifiers and phase lock loops. Chapter eight concerns analog-to-digital and digital to analog converter principles. Chapter Nine deals specifically with interconnect, with information on the propagation delay and crosstalk effects. The input/output interfacing principles are illustrated in Chapter 10.

The detailed explanation of the design rules is in appendix A. The program operation and the details of all commands are given in appendix B. A quick reference sheet is reported in appendix C.

Etienne SICARD

Toulouse, September 2000

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- *Matra Systems et Information, Toulouse, France (<http://emc2000.matra-ms2i.com>)*
- *ST-Microelectronics, Crolles, France (<http://www.st.com>)*