COURSE DATA

DATA SUBJECT

Code: 34803
Name: Digital systems I
Cycle: Undergraduate Studies
ECTS Credits: 6
Academic year: 2026-27

STUDY (S)

Degree	Center	Acad. year	Period
1402 - Degree in Telecommunications Electronic Engineering	Escola Tècnica Superior d'Enginyeria	1	Second quarter

SUBJECT-MATTER

Degree	Subject-matter	Character
1402 - Degree in Telecommunications Electronic Engineering	Digital electronic systems	COMPULSORY

COORDINATION

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SUMMARY

The course 'Digital Electronic Systems I' (Sistemas Electrónicos Digitales I) is the first of several courses related to digital electronic systems. The main objective for this course is the study of the basic techniques for the analysis and design of digital systems, setting up the basic knowledge and easing the study of complex systems to be covered in further courses.

This is a compulsory course taught in the first year of the Telecommunication Electronic Engineering degree (GIET) during the second semester (spring semester). This course has a length of 6 ECTS from which 3 ECTS correspond to theory classes, 1 ECTS for problem solving classes and 2 ECTS for laboratory sessions.

This course covers a global vision of digital systems inside the field of digital electronic systems. The proposed topics will allow the student to design a basic digital system and analyse the requirements needed for implementing a digital design. In order to achieve these goals, the students will learn about different digital systems such as combinational and sequential subsystems, timing circuits, basic digital integrated circuits, programmable logic circuits, etc.

This is a practical course. The principles of digital design are accompanied with examples. Students will

perform frequent exercises, both for analysis and design of digital systems, which will further test and create in the laboratory.

As a summary, this course provides a basic foundation for design and analysis of digital electronic systems and their associated circuits.

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PREVIOUS KNOWLEDGE

RELATIONSHIP TO OTHER SUBJECTS OF THE SAME DEGREE

There are no specified enrollment restrictions with other subjects of the curriculum.

OTHER REQUIREMENTS

This course is self-contained and does not require any previous knowledge as it is one of the first courses related to electronics and they do not have previous knowledge in the field.

COMPETENCES / LEARNING OUTCOMES

1402 - Degree in Telecommunications Electronic Engineering

Capacidad de análisis y diseño de circuitos combinacionales y secuenciales, síncronos y asíncronos, y de utilización de microprocesadores y circuitos integrados.

G3 - Acquisition of the knowledge of the basic and technological subjects that allows students to learn new methods and theories and endows them with the versatility to adapt to new situations.

G4 - Ability to solve problems with initiative, decision-making and creativity, and to communicate and transmit knowledge, abilities and skills, understanding the ethical and professional responsibility of the activity of a telecommunications technical engineer.

R10 - Understand and apply the fundamentals of hardware description languages describing hardware devices.

DESCRIPTION OF CONTENTS

0. Introduction to numeration systems and binary arithmetic

Numeral systems
Arithmetic operation in binary code
Binary signed numbers
Binary fixed-point and floating point numbers

BCD code
Alphanumeric coding

1. Boole¿s algebra. Logic gates. Boolean functions simplification. Logic families.

Analog and digital signals: digital processing
Boole¿s Algebra
Logic gates and Logic functions
Logic function simplification
Logic Families

2. VHDL description language and logic simulation

General introduction to simulation and hardware description languages (HDL)
Pros and cons of using HDLs
Basic elements and data types in VHDL
Sequential and concurrent statements in VHDL
Testbenches
Simulation

3. MSI combinational circuits

Multiplexers and Demultiplexers
Encoders and Decoders
Code converters
Comparator circuits
Arithmetic circuits. Arithmetic-Logic Units (ALU)

4. Bistable circuits: Flip-flops and Latches

Introduction
Bistable R S: funcionamiento síncrono y asíncrono
Bistable J K
Bistable T
Bistable D
Considerations in the design with bistables using VHDL
Parameters in bistables

5. Sequential circuits

Definition. Shift registers
Asynchronous counters

Synchronous counters
Other counters: up-down, ring, Johnson
Counters in VHDL

6. Digital circuits for clock and timer generation

Schmitt Trigger gates
Timing circuits using logic gates.
Digital Timing circuits
Clock generation using logic gates
Astable digital circuits

7. State machine design

Mealy and Moore state machines
Analysis of synchronous sequential circuits
Synthesis of State machines
VHDL Description for Mealy and Moore state machines

8. FPGA and programmable logic devices

Programmable Logic Devices (PLD): FPGA and others
FPGA global market
Tecnologies
Applications

WORKLOAD

PRESENCIAL ACTIVITIES

Activity	Hours
Theory	30,00
Laboratory	20,00
Classroom practices	10,00
Total hours	**60,00**

NON PRESENCIAL ACTIVITIES

Activity	Hours
Attendance at other activities	0,00
Individual or group project	0,00
Independent study and work	35,00
Preparation of lessons	29,00
Preparation for assessment activities	11,00
Resolution of case studies	10,00

Total hours	**85,00**

TEACHING METHODOLOGY

The course is organised around three types of attending classes: theory classes, problem solving classes and laboratory classes. Office hours are used as additional tool for students. Concerning out-of-classroom activities, additional exercises must be solved, as well as preparation of upcoming lectures and consolidating previous contents taught.

In theory and problem-solving classes, traditional teaching method will be used. In theory sessions the teacher will explain the basic contents of the course using different teaching tools as slide presentation, together with other tools (G3,G4,R9,R10). Problem-solving classes will use two different models. First, the teacher will propose and solve different problems which are essential for understanding of digital systems from students, learning to follow a design procedure and identifying the required elements needed to adequately solve a problem (G3,G4,R9,R10). Second, the teacher will propose a problem and the students must solve the problem being distributed into groups, individually, or using other group working techniques and always under direct supervision of the teacher (G4,R9); once completed, the solutions will be collected by the teacher and corrected by the teacher or the students (depending on the case).

Students have a specific office-hour calendar where the teacher is available in the office for any concern related to the course (problem solving, theory doubts, report guidance, etc.). The attending hours will be detailed at the beginning of the academic year. Additionally, there exist a remote 'office-hours' program where questions can be solved using e-mail contact. The use of the students' portal 'Aula Virtual' provided by the University of Valencia is encouraged, where all the information related to the course is available online.

Laboratory sessions are organized according to three basic principles: design, mounting (real or virtual mounting) and testing/simulating electronic digital systems (G4,R9,R10). The estimated duration for each laboratory session is 3 hours. The session will be carried out by groups of, at most, two persons. The student will get the laboratory activities' guide in advance so that previous preparation time is allowed. Once in the laboratory, there exists a direct supervision from the teacher. The student must assume the responsibility for all the stages in the proposal: design, mounting/simulating, and testing. The final goal of the laboratory is to obtain a working system according to initial specifications. Finally, a lab report will be required from the teacher (G3,G4,R9,R10).

All of the described activities will be always using the support of 'Aula Virtual' as the most important source of information and communication for the student.

EVALUATION

Assessment of student learning will take place following two models:

MODEL A

By continuous assessment tests from the theoretical sessions and problems, plus the scores obtained in lab sessions. To qualify for this type of evaluation, the student must regularly attend classes and theoretical problems and be active in the dynamics of cooperative work. To average the exam scores of theory and laboratory, it is required that each of them is equal or higher than 4. The final grade is obtained from the following considerations:

¿ The theory mark will emerge as a result of a written exam, done on the dates indicated in the oficial calendar for first call. It will consist of different questions of theoretical and practical problems (G3,G4,R9, R10). All questions will be related to the contents of the agenda, and with similar issues and problems done in class difficulty. This classification corresponds to 35% of the final grade (Ex_Teoria).

¿ Upon completion of the course, a multiple-choice test that will count for 20% of the final grade will be made (G3,G4,R9,R10) (Ex_Test). Alternatively, other activities can be proposed, according to the teacher's criteria.

¿ The laboratory note is a result of the realization of an individual exam at the end of the semester, which will include a number of issues directly related to the practices done during the course (G3,G4,R9,R10). It will consist of the design, assembly and / or simulation of some of the sections made by students throughout the laboratory sessions they attended during the course. Demonstrated skills, proficiency in the use of laboratory equipment and design development throughout the session will be assessed. It is a prerequisite to regularly attend lab sessions (you cannot miss more than 1 session). This note is equal to 25% of the final grade (Ex_Lab).

¿ In addition, each lab sessions is assessed using a few simple questions at the beginning and end of each session (G3,G4,R9,R10). This ongoing evaluation of the work done by students in all lab sessions consider skill, interest and results. This assessment translates into 20% of the final grade for the course (Eval_Lab).

The final grade for the course will come from the following expression:

Final_Score = (0,35*Ex_Teoria)+(0,25 * Ex_Lab)+(0,2*Eval_Lab) + (0,2 * Ex_Test)

MODEL B

In this mode, the exam will consist of a theoretical part, in which the student must demonstrate knowledge of the concepts and relationships seen in class and a second part which is a laboratory test (G3,G4,R9, R10). In this, the students must complete the design, assembly and / or simulation of specified digital systems related to the contents of the agenda and with similar issues and practices developed in the laboratory scripts difficulty (G3,G4,R9,R10). To average the test scores of theory and laboratory will require each of them to equal or exceed 4. The final grade for the course will leave the following expression:

Final_Score = (0,55*Ex2_Teoria)+(0,25 * Ex2_Lab)+(0,20*Eval_Lab)

Initially, all students will follow evaluation model A, and, in case of failing the course, they will follow model B. In case of partial passing the exams in model A, the student can only repeat the exam in the second call with score under 4. The passed score obtained in model A will be used to obtain the final score in model B.

The score obtained in laboratory sessions (Eval_Lab) cannot be repeated and the same score will be used for both models.

In any case, the final score must be equal or above 5 for passing the course.

¿In any case, the evaluation system will be governed by what is established in the Evaluation and Qualification Regulations of the Universitat de València for Degrees and Masters (https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639)¿.

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