

**COURSE DATA****DATA SUBJECT****Code:** 34825**Name:** Hardware implementation of digital signal processing systems**Cycle:** Undergraduate Studies**ECTS Credits:** 6**Academic year:** 2026-27**STUDY (S)**

Degree	Center	Acad. year	Period
1402 - Degree in Telecommunications Electronic Engineering	Escola Tècnica Superior d'Enginyeria	4	Second quarter

**SUBJECT-MATTER**

Degree	Subject-matter	Character
1402 - Degree in Telecommunications Electronic Engineering	Optional subjects	ELECTIVES

**COORDINATION**

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**SUMMARY**

The subject "Hardware Implementation Systems Digital Signal Processing", 6 ECTS, taught in the second semester of Electronics Engineering Degree in Telecommunications (GIET). Part of the matter, "Signals, Systems and Telecommunication Services", is optional and is taught by faculty from the Department of Electronic Engineering.

In the course there are two distinct parts, although they focus on the implementation of systems in hardware devices. In the first part provides students with a deeper content in the field of programmable logic, both from the standpoint of hardware and software. Architectures are described generation devices and their manufacturing technologies and applications. It delves into the hardware description language VHDL for modeling and design of digital electronic circuits and describes oriented VHDL synthesis. Be reviewed in detail the study and implementation of sync timing constraints for the proper functionality of the designs. The second part introduces Digital Signal Processors, as a tool for digital signal processing in real time. It describes the basic elements of a system of this nature, development tools and proceeds to implement practical examples of processing algorithms (digital filtering, frequency analysis, etc.)



The content must allow a student to approach the design of a digital system being able to analyze a application that requires this type of design.

This is an eminently practical subject in which, after the introduction of the concepts, students will undertake numerous practical exercises, mainly design digital systems based on FPGAs and DSPs, as well as laboratory experimentation.

The objectives of this course are summarized in the following points:

- Designing a system properly based digital programmable logic.
- Use proper hardware description languages  $\mathcal{L}$  for programmable logic device programming.
- Choose properly a programmable logic device meeting the requirements of design and devices on the market.
- Plan properly the overall structure of a digital system and the interplay between its different elements.
- Estimate reliably the functional delay of a digital system for the proper synchronization with other external and / or internal functional module.
- Getting to the development board and tool TMS320C6713 Code Composer Studio development.
- Breaking the barrier between the theoretical contents of digital signal processing and its practical implementation in real time.
- Implementation of digital processing blocks of real time.

The contents of the course are:

High density programmable devices. PSoC devices. VHDL hardware description language. VHDL synthesis oriented. Basic architecture of a Digital Signal Processor. Programming Tools: Code Composer. Implementation of applications.

## PREVIOUS KNOWLEDGE

## RELATIONSHIP TO OTHER SUBJECTS OF THE SAME DEGREE

There are no specified enrollment restrictions with other subjects of the curriculum.

## OTHER REQUIREMENTS

Successfully addressing this subject is recommended that the student possesses prior knowledge acquired in the subjects of Electronic Circuits and Digital Systems I, II, Signals and Linear Systems and Digital Signal Processing. Such prior knowledge include:

- Numbering Systems
- Boolean algebra
- Maxterms, minterms and a logic function.
- Simplification of logical functions: Karnaugh methods and Quine-McCluskey



- Combinational and Sequential Subsystems.
- Design of state machines.
- Sampling and reco

## COMPETENCES / LEARNING OUTCOMES

## DESCRIPTION OF CONTENTS

### 1. Technologies and devices for hardware implementation: Programmable Logic and Systems

Introduction. Classification. Types. ALTERA programmable devices: classic family, MAX and FLEX. XILINX Programmable Devices: family of CPLDs and FPGAs. Other devices (Lattice, Actel, etc..). Introduction to PSoC. Cypress Family devices. Development Software PSoC Designer IDE.

### 2. Algorithmic State Machines

Introduction. Definition. ASM Charter. Design of the control unit. Design of de processing unit. Design methodology. Examples.

### 3. VHDL hardware description language

VHDL structural elements. Predefined data types and type definitions themselves. Sequential and concurrent sentences. Defining libraries. Subprograms. Test benches.

### 4. Synthesis oriented VHDL language

General considerations on the synthesis process. Synthesizable VHDL subset (sequential logic combinational finite state machines, generating high impedance, etc.. General design recommendations.

### 5. Digital signal processors

Introduction. Description of digital signal processors. Types of DSPs. Definition of real time. Applications

### 6. DSK 6713 development system

Introduction to DSK6713 development system. Devel tools: Code Composer Studio. Programs. Examples.



## 7. Implementation of processing systems

Signal generation implementing FIR filters, IIR filter implementation, fast Fourier transform, adaptive filters: Application Examples.

## 8. Laboratory Practices

- LAB SESSION 1: VHDL Description of Combinational Systems: synthesis and hardware implementation CoolRunner-II CPLD. (3h)
- LAB SESSION 2: Sequential Systems VHDL description and state machines: synthesis and hardware implementation CoolRunner-II CPLD. (3.5h)
- LAB SESSION 3: VHDL description of a digital system: synthesis and hardware implementation CoolRunner-II CPLD. (3.5h)
- LAB SESSION 4: Design of digital filters in Matlab and implementation in real time on the DSP board: application to FIR filtering of audio signals. (3.5h)
- LAB SESSION 5: Detection of DTMF frequencies using Goertzel algorithm and IIR filtering. (3.5h)
- LAB SESSION 6: Practical application of real-time processing: electrocardiogram analysis. (3.5h)

## WORKLOAD

### PRESENCIAL ACTIVITIES

Activity	Hours
Theory	40,00
Laboratory	20,00
<b>Total hours</b>	<b>60,00</b>

### NON PRESENCIAL ACTIVITIES

Activity	Hours
Attendance at other activities	0,00
Individual or group project	0,00
Independent study and work	13,00
Preparation of lessons	52,00
Preparation for assessment activities	25,00
Resolution of case studies	0,00
<b>Total hours</b>	<b>90,00</b>

## TEACHING METHODOLOGY

The training activities are developed according to the following distribution:

### Theoretical activities



Description: In the lectures will develop the issues by providing a comprehensive and integrative, analyzing in detail the key issues and more complex, promote, at all times, the student's participation.

### Practical activities

Description: Complement theoretical activities in order to apply the basic concepts and expand the knowledge and experience they acquire during the course of the work proposed. They include the following types of classroom activities:

- Classes of problems and issues in classroom
- Sessions for discussion and resolution of problems and exercises previously studied by students
- Labs.

It will use the e-learning platform (LMS) of the University of Valencia in support of communication with students. Through it you will have access to course materials used in class, as well as solving problems and exercises.

## EVALUATION

The subject will be evaluated in two halves, corresponding to the half of the subject with content of FPGAs and half with the content of DSPs. Each part will count 50% of the final grade, and for each half the grade will be calculated as described below.

In the first call, the subject will be evaluated using one of the following two possibilities:

1.- Through the continuous evaluation of the laboratory sessions (TE5, R2, R9, R10) and the realization of a certain number of proposed tasks (TE5, R2, R9, R10). The percentages according to this type of evaluation will be the following:

- 60% Evaluation of laboratory sessions
- 40% Assessment of tasks

2.- Through the realization of a theoretical-practical examination at the end of the course (TE5, R2, R9, R10), by means of the continuous evaluation of the laboratory sessions (TE5, R2, R9, R10 ) and from the performance of one or more tasks (TE5, R2, R9, R10). In order to average the marks, it will be necessary that the mark of the theoretical examination is equal or superior to 5. The percentages according to this modality of evaluation will be the following:



- 30% Theoretical exam.
- 50% Evaluation of laboratory sessions.
- 20% Assessment of tasks.

In the second call, the subject will be evaluated through the realization of a theoretical-practical exam that will have a weight of 100%.

In any case, the evaluation system will be governed by the provisions of the Regulations for the Evaluation and Qualification of the University of Valencia for Degrees and Masters

Copying or plagiarism of any activity that is part of the evaluation will result in the impossibility of passing the course, and the student will then be subject to the appropriate disciplinary procedures indicated in the ACTION PROTOCOL FOR FRAUDULENT PRACTICES AT THE UNIVERSITY OF VALENCIA ([ACGUV 123/2020](#))

<https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639>).

## REFERENCES

- Xilinx Devices. [http://www.xilinx.com/products/silicon\\_solutions/](http://www.xilinx.com/products/silicon_solutions/)
- Floyd, T.L. "Fundamentos de Sistemas Digitales.". Prentice Hall, 2007.
- Machado, F.; Borromeo, S.; Malpica, N. ¿Diseño Digital Avanzado con VHDL (Vol. 1)¿. Colección Textos Docentes Universidad Rey Juan Carlos, 2009
- Thad B.Welch, Cameron H.G.Wright, Michael G. Morrow. Real Time Digital Signal Processing from MATLAB to C with the TMS320C6X DSPs (segunda edición). CRC Press. 2012
- R. Chassaing and D. Reay, Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK. ,2nd ed.Hoboken NJ: John Wiley & Sons, 2008, pp. 576. ISBN: 9780470138663 (Disponible e-libro
- S.M. Kuo, B.H. Lee, W. Tian, Real-time digital signal processing : implementations and applications, 2 ed. John Wiley, 2007. ISBN:9780470014950
- Altera Devices. <http://www.altera.com/products/devices/dev-index.jsp>
- Pardo, F.; Boluda, J. A.; "VHDL: Lenguaje para síntesis y diseño de circuitos digitales". Ed. Rama, 1999.
- Proakis, John G. Tratamiento digital de señales / John G. Proakis, Dimitris G. Manolakis Madrid [etc.] : Pearson-Prentice Hall, 2007