# COURSE DATA

## DATA SUBJECT

**Code:** 34837
**Name:** Computer structure
**Cycle:** Undergraduate Studies
**ECTS Credits:** 6
**Academic year:** 2025-26

## STUDY (S)

| Degree | Center | Acad. year | Period |
|---|---|---|---|
| 1407 - Degree in Multimedia Engineering | Escola Tècnica Superior d'Enginyeria | 2 | First quarter |

## SUBJECT-MATTER

| Degree | Subject-matter | Character |
|---|---|---|
| 1407 - Degree in Multimedia Engineering | Ingeniería de Computadores | COMPULSORY |

## COORDINATION

BOLUDA GRAU JOSE ANTONIO

# SUMMARY

The course "Computers Structure" is a core course of the second year of the Multimedia Engineering Degree. The course workload is 6 ECTS and it is given in the first four-month period of the second year. This course is a part of the subject "Computer Engineering" of the Multimedia Engineering Degree curriculum.

The course "Computer Structure" deals with the Von Neumann computer architecture. During this course, the presentation of the elementary computer structure, which it was started in the first year course "Fundamental of Computers", is completed. "Fundamental of Computers" is focused on the microprocessor architecture and machine language. Following the Von Neumann computer structure, this course continues the study introducing the rest of its internal components (memory, buses and input / output system) and the computer peripherals.

The first section of the course is focused on the hierarchical memory system. At the beginning of this

section, various memory technologies that can be used to build the computer memory system are presented. It is intended that students know their capabilities in terms of performance, capacity and cost. Then, the main memory and its internal organization are introduced. Once the students have learnt how to build a memory system, the hierarchical design is presented as the logical solution to the optimization of memory system design under capacity, performance and cost constraints. Cache memory is located at the higher level of the hierarchical system. The student must understand the cache structure, its design parameters, operation policies and its impact on the system performance. Finally, this section ends with the description of the virtual memory that automatically handles the exchange of information between the two lower levels in the hierarchy, i.e.: main memory and secondary storage. The virtual memory completes the presentation of the hierarchical memory system. One of the most important competences that students should gain during this course is the understanding of the combined operation of the three memory levels and how to evaluate the performance.

In the second section of the course, the student will gain understanding of how the process of exchanging information between the computer and peripherals is performed. The contents of this section include the system input / output structure and the data transactions. The student should be able to determine the best method to carry out and manage the data transactions depending on the peripheral, whether based on polling, interruption or by DMA. Finally, this section finishes presenting the internal buses. These elements interconnect all the computer internal components and allow the information exchange between them. Students will learn the structure of the current buses and the way the data is transferred.

The following section of the course provides a basic knowledge of the most common computer peripherals and their operation. It begins with data input devices i.e.: keyboard, mouse, etc. Then it moves on to study the mass storage and RAID technologies and the problems associated with the sequential data access and the way in which the information is organized. Finally, video terminals complete the contents of this part.

The last block is focused on a brief presentation of parallel computer architectures. First, it is introduced a classification of different architectures according to the way in which the data processing is performed and the degree of coupling in the execution of programs. After that, several advanced techniques applied to conventional computers are explained, i.e. segmentation and superscalar processors. Then, systems running the same program on multiple data, such as vector and matrix processor, and multicomputer and multiprocessor architectures are introduced. Finally, the section ends with some examples of specific architectures, such as: GPUs for graphics processing.

## PREVIOUS KNOWLEDGE

### RELATIONSHIP TO OTHER SUBJECTS OF THE SAME DEGREE

There are no specified enrollment restrictions with other subjects of the curriculum.

### OTHER REQUIREMENTS

It is advisable to have attended the courses corresponding to the subject "Informatics".

## COMPETENCES / LEARNING OUTCOMES

### 1405 -

B4 - Have basic skills in the use and programming of computers, operating systems, databases and computer software for use in engineering.

G3 - Take into account the economic and social context in engineering solutions, be aware of diversity and multiculturalism and ensure sustainability and respect for human rights and equality between men and women.

I2 - Know, design and make an efficient use of the data types and data structures that are most suited to solving a problem.

I5 - Know the features, functionalities and structure of operating systems and be able to implement applications based on their services.

MM1 - Have knowledge and ability to understand essential facts, concepts, principles and theories related to multimedia systems including all the disciplines covered by these systems.

MM2 - Be able to understand and manage the different technologies involved in multimedia systems, both from the point of view of hardware and electronics and of software.

MM3 - Be able to implement methodologies, technologies, processes and tools for the professional development of multimedia products in a real context of use by applying the appropriate solutions for each environment.

MM5 - Know how to apply the theoretical and practical resources to deal with a multimedia application as a whole.

## DESCRIPTION OF CONTENTS

1. Memory Hierarchy

Technologies of the integrated circuits that form the main memory
Main memory organization
Design of the hierarchical memory system
Cache memory
Mapping algorithms for cache memory
Benefits of cache memory
Virtual Memory

2. Communications between processor and peripheral devices

Input/Output Modules
Synchronization by polling and interrupt
Direct Memory Access (DMA)

3. Buses and Interfaces

Features of a bus
Types of transfers
Examples of Buses

4. Peripheral devices

Input devices
Data Storage Systems
Video Terminals

5. Advanced architectures

Introduction and classification of parallel systems
Advanced conventional architectures
Vector and matrix processors
Shared memory multiprocessors
Distributed memory systems
Examples: GPU

## WORKLOAD

### PRESENCIAL ACTIVITIES

| Activity | Hours |
|---|---|
| Theory | 30,00 |
| Laboratory | 20,00 |
| Classroom practices | 10,00 |
| **Total hours** | **60,00** |

### NON PRESENCIAL ACTIVITIES

| Activity | Hours |
|---|---|
| Attendance at other activities | 0,00 |
| Individual or group project | 10,00 |
| Independent study and work | 10,00 |
| Preparation of lessons | 25,00 |
| Preparation for assessment activities | 25,00 |
| Resolution of case studies | 20,00 |

| | |
|---|---|
| Total hours | 90,00 |

## TEACHING METHODOLOGY

**Theoretical activities.**

Description: The lectures will present the course contents providing a global vision, a detailed analysis of the key concepts and encouraging the student participation. The workload of this section for the students is 19% of the total of the course.

**Practical activities.**

Description: The practical activities complement the theoretical classes and allow the students to put into practice the contents and improve the understanding of the course concepts. They include the following types of classroom activities:

• Solving problems in class.
• Regular discussion of exercises and problems that the students have previously tried to work out.

• Laboratory sessions.

• Oral presentations.

• Support tutorial sessions (individualized or in group).

• Individual evaluation of questionnaires to be done in class with the help of teachers.

The workload of this section for the students is 21% of the total of the course.

**Personal work.**

Description: It is the work that the student must carry out individually out of the classroom timetable. It tries to promote the autonomous work habit. Activities in this group are: monographs, guided literature search, exercises and problems as well as preparation of classes and exams. The workload of this section for the students is 45% of the total of the course.

**Teamwork in small groups.**

Description: It will be carried out by small groups of students (2-4). It consists of work to be done out of the class timetable in form of exercises and problems. This work tries to improve the teamwork and leadership skills. The workload of this section for the student is 15% of the total charge of the course.

During the course the e-learning (pizarra virtual) platform of the University of Valencia will be used to support the teaching activities. This platform allows the access to the course materials used in the classes as well as additional documents, solved problems and exercises.

## EVALUATION

The subject evaluation will be carried out in the first call preferably through continuous evaluation tests (C) and the evaluation of the laboratory activities (L). All these activities, controls and laboratory sessions, cannot be make up.

The continuous assessment grade (C) will be calculated as the weighted average of two continuous assessment tests carried out during the course (P*), at the end of each thematic block or group of subjects: P1 and P2. The following expression will be used, which reflects the relative weight of each thematic block:

$C = 0.6 * P1 + 0.4 * P2$

If the continuous evaluation grade is greater than or equal to 5, the student will not have to take the official exam of the 1st call, calculating the grade of the 1st call (N1a) as:

$N1a = 0.8 * C + 0.2 * L$

Where the laboratory grade (L) will be calculated as the arithmetic mean of the evaluation of the laboratory sessions.

If C is minor than 5, there will be no N1a grade, and the official exam of the 1st call (Ex1) will have to be taken, calculating the grade of the 1st call differently (N1b):

N1b = 0.7 * Ex1 + 0.2 * L + 0.1 * C

In the case of any student who has passed the continuous assessment and wants to improve his grade N1a, he can take the Ex1 exam, calculating the grade of the 1st call with the two methodologies and staying with the highest, N1a or N1b.

The grade of the 2nd call (N2) will be calculated in a single way, based on the exam grade of the 2nd call Ex2 and with the laboratory (L) and continuous assessment (C) grades obtained during the course. Notes L and C are not recoverable.

N2 = 0.7 * Ex2 + 0.2 * L + 0.1 * C

Copying or plagiarism of any activity that is part of the evaluation will result in the impossibility of passing the course, and the student will then be subject to the appropriate disciplinary procedures indicated in the ACTION PROTOCOL FOR FRAUDULENT PRACTICES AT THE UNIVERSITY OF VALENCIA (ACGUV 123/2020).

In any case, the evaluation of this subject will be done in compliance with the University Regulations in this regard, approved by the Governing Council on 30th May 2017 (ACGUV 108/2017)

## REFERENCES


- Estructura y diseño de computadores. Patterson, D.A. y Hennesy, J. 4th Edition on line. Ed. Morgan Kaufmann (2012): https://www.dawsonera.com/abstract/9780080886138 3rd Edition

on line. Ed. Morgan Kaufmann (2007): http://site.ebrary.com/lib/universvaln/detail.action?docID=10382827

- Organización y arquitectura de computadores. 7ª Edición. Stallings, William. Prentice Hall, 2006. On Line: http://www.ingebook.com/ib/NPcd/IB_BooksVis?cod_primaria=1000187&codigo_libro=1266

- Estructura de computadores y periféricos Rafael Martínez Durá, José A. Boluda Grau, Juan José Pérez Solano. Rama. 2002

- Fundamentos de los Computadores. Novena Edición. P. de Miguel Anasagasti. Ed. Thomson. 2004

- Computer periphericals. Barry Cook y Neil White. Edward Arnold, 3ª edición. 1995