COURSE DATA

DATA SUBJECT

Code: 34883
Name: Digital systems II
Cycle: Undergraduate Studies
ECTS Credits: 6
Academic year: 2026-27

STUDY (S)

Degree	Center	Acad. year	Period
1403 - Degree in Telematics Engineering	Escola Tècnica Superior d'Enginyeria	2	Second quarter
1935 - Double Degree Program in Mathematics-Telematics Engineering	Facultat de Ciències Matemàtiques	3	Second quarter

SUBJECT-MATTER

Degree	Subject-matter	Character
1403 - Degree in Telematics Engineering	Digital electronic systems	COMPULSORY
1935 - Double Degree Program in Mathematics-Telematics Engineering	Tercer curso	COMPULSORY

COORDINATION

PEREZ SOLANO JUAN JOSE

SUMMARY

The course "Digital Electronic Systems II" is a core course of the second year of Bachelor¿s Degree in Telematics Engineering. The course workload is 6 ECTS and it is given in the first four-month period of the second year. This course is a part of the subject "Digital Electronic Systems" of the Telematics Engineering Degree curriculum.

The main goal of "Digital Electronic Systems II" is to provide students with the understanding of the basic structure of a computer and how to design digital electronic systems based on microprocessors. The first section of this course introduces the computer language, i.e. machine language, presenting the computer instruction set, the formats of the instructions and the operands addressing modes. Once the generic concepts about machine language are provided, the study is focused on the presentation of the MIPS32 microprocessor instruction set.

The next goal is the understanding of the basic computer components and their role in the development of the computer architecture. In this section, the student will be able to design the data paths inside the

computer and the control unit that manages the overall operation. The arithmetic-logic unit (ALU) is studied with the aim that students can understand how basic operations are performed in the computer and how to design it correctly.

The following section treats the hierarchical computer memory system. First of all, various memory technologies that can be used to build the computer's memory system are introduced. It is intended that students know their capabilities in terms of performance, capacity and cost. Then, the concept of main memory and its internal organization is introduced. Students will learn how to design a small memory system and specify the memory map of a computer. Finally, the student is faced with the problem of optimizing the memory design under capacity, performance and cost constraints, and its solution based on a hierarchical design with three different levels: cache, main memory and virtual memory.

In the next section of the course the student will gain understanding of how the exchange of information between the computer and peripherals is performed. The input/output system structure and the transfer of information will be presented. The student should be able to determine the best method to carry out a data transfer between a computer and a peripheral, whether based on polling or interrupts. The presentation of the internal structure of the computer finishes dealing with the internal bus that interconnects all the computer components and performs the exchange of information between them.

The last section of the course is focused on the design of microcontroller-based systems. In this section the microcontroller structure and the most popular families of this type of devices are introduced. After that, the PIC32 microcontroller, based on the MIPS32 architecture, will be presented in detail. Finally, most common integrated peripherals are showed: timers, analogue to digital converters and communications modules, jointly with the development of applications using high level programming languages.

PREVIOUS KNOWLEDGE

RELATIONSHIP TO OTHER SUBJECTS OF THE SAME DEGREE

There are no specified enrollment restrictions with other subjects of the curriculum.

OTHER REQUIREMENTS

It is advisable to have attended the courses corresponding to the subject "Circuitos y componentes electrónicos y fotónicos".

COMPETENCES / LEARNING OUTCOMES

1403 - Degree in Telematics Engineering

G3 - Acquisition of the knowledge of the basic and technological subjects that allows students to learn new methods and theories and endows them with the versatility to adapt to new situations.

G4 - Ability to solve problems with initiative, decision-making and creativity, and to communicate and transmit knowledge, abilities and skills, understanding the ethical and professional responsibility of the activity of a telecommunications technical engineer.

R9 - Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous, and use microprocessors and integrated circuits.

DESCRIPTION OF CONTENTS

1. Machine language.

- Introduction to computer architecture.
- Types and formats of instructions.
- Operands addressing modes.
- The particular case of RISC-V.

2. Processor internal structure.

- Datapath and control signals.
- Control unit design.
- Pipelining.

3. Memory hierarchy.

- Main memory system design.
- Memory maps.
- Hierarchical memory system design.

4. Input /output system.

- I/O modules and controllers.
- Interrupts

WORKLOAD

PRESENCIAL ACTIVITIES

Activity	Hours
Theory	30,00
Laboratory	20,00
Classroom practices	10,00
Total hours	**60,00**

NON PRESENCIAL ACTIVITIES

Activity	Hours
Attendance at other activities	0,00
Individual or group project	0,00
Independent study and work	20,00
Preparation of lessons	30,00
Preparation for assessment activities	20,00
Resolution of case studies	20,00
Total hours	**90,00**

TEACHING METHODOLOGY

All the teaching activities of the course are focused on the achievement of the R9 competence.

The teaching activities will be developed according to the following distribution:

The 40% of workload of the course in ECTS (1 credit corresponds to 25 hours) will be spent in the following in class activities:

Theoretical activities.

Description: The lectures will present the course contents providing a global vision, with a more detailed analysis of the key aspects and the more complicated concepts and encouraging the student participation.

Practical activities.

Description: The practical activities complement the theoretical classes and allow the students to put into practice the course contents and improve its understanding through the knowledge and experience gained during the achievement of the proposed work. They include the following types of classroom activities:

• Solving problems in class.

• Regular discussion of exercises and problems that the students have previously tried to work out.

• Laboratory sessions.

• Oral presentations.

• Support tutorial sessions (individualized or in group).

• Individual evaluation of questionnaires to be done in class with the help of professors.

Assessment:

Description: Students will carry out individual examinations in class and in the presence of professors.

The 60% of workload of the course in ECTS (1 credit corresponds to 25 hours) will be spent in the following out of class activities:

Personal work.

Description: It is the work that the student must carry out individually out of the classroom timetable. It tries to promote the autonomous work. Activities in this group are: monographs, guided literature search, exercises and problems as well as preparation of classes and exams.

Teamwork in small groups.

Description: It will be carried out by small groups of students (2-4). It consists of work to be done out of the class timetable in form of exercises and problems. This work complements the individual work and tries to improve the teamwork and leadership skills.

During the course the e-learning (pizarra virtual) platform of the University of Valencia will be used to support the teaching activities. This platform allows the access to the course materials used in the classes as well as additional documents, solved problems and exercises.

EVALUATION

The course evaluation will be performed preferably by the continuous assessment mark (C) and the laboratory mark (L).

The continuous assessment mark (C) is calculated as the weighted average of 2 continuous assessment tests, taken during the course, at the end of each group of course sections: P1 and P2. The following expression will be used, which reflects the relative weight of each part:

$$C = 0,6 * P1 + 0,4 * P2$$

If the continuous assessment mark (C) is greater or equal than 5 the student may not take the official first examination of the course, calculating the grade of the course as:

$$N1a = 0,8 * C + 0,2 * L$$

Where the laboratory mark (L) is calculated as the average of the laboratory sessions marks.

The continuous assessment mark (C) and laboratory mark (L) can not be retaken and these marks will be maintained at the first and the second exam sittings.

If C is lower than 5 the student must take the official first examination (Ex1), calculating the grade of the course as:

$$N1b = 0,8 * maximum\{C , Ex1\} + 0,2 * L$$

If a student, who has passed the continuous assessment with a mark higher or equal to 5 (C is higher tahn 5), wants to improve its final grade N1a, he/she may take the examination Ex1.

At the second exam sittings, the grade (N2) is calculated using the official second examination mark (Ex2), the laboratory marks (L) and continuous assessment mark (C). The final grade of the course in this case is calculated as:

$$N2 = 0,8 * maximum\{C , Ex2\} + 0,2 * L$$

Copying or plagiarism of any activity that is part of the evaluation will result in the impossibility of passing the course, and the student will then be subject to the appropriate disciplinary procedures indicated in the ACTION PROTOCOL FOR FRAUDULENT PRACTICES AT THE UNIVERSITY OF VALENCIA (ACGUV 123/2020).

In any case, the assessment shall conform to the "**Reglament d'avaluació i qualificació de la Universitat de València per a títols de grau i de màster"** approved by the Governing Council of the UVEG on May 30, 2017. It states basically that the final grade will be numbered from 0 to 10 with a decimal expression and a qualitative rating scale will be added following this guideline:

• From 0 to 4.9: "Failed"
• From 5 to 6.9 "Approved"
• From 7 to 8.9, "Notable"
• From 9 to 10: "Excellent" or "Honors with Distinction"

n"

REFERENCES

- Computer Organization and Design RISC-V Edition. Patterson, D.A. y Hennesy, J. Reverté, Morgan Kaufmann. https://trobes.uv.es/permalink/34CVA_UV/1bttdu2/alma991010250003706258.
- Computer Organization and Architecture. William Stallings. 10ª ed. Pearson.
- RISC-V Assembly Language Programming : Unlock the Power of the RISC-V Instruction Set. Stephen Smith. 1º ed. Apress. https://trobes.uv.

es/permalink/34CVA_UV/1bttdu2/alma991010395463206258

- ESP32-C3 Hardware Reference (Web Espressif) https://docs.espressif.com/projects/esp-idf/en/stable/esp32c3/hw-reference/index.html