COURSE DATA

DATA SUBJECT

Code: 34936
Name: Digital systems I
Cycle: Undergraduate Studies
ECTS Credits: 6
Academic year: 2026-27

STUDY (S)

Degree	Center	Acad. year	Period
1404 - Degree in Industrial Electronic Engineering	Escola Tècnica Superior d'Enginyeria	3	First quarter, Sin determinar

SUBJECT-MATTER

Degree	Subject-matter	Character
1404 - Degree in Industrial Electronic Engineering	Electronic systems	COMPULSORY

COORDINATION

BATALLER MOMPEAN MANUEL

SUMMARY

The course 'Digital Electronic Systems I' (Sistemas Electrónicos Digitales I) is the first of several courses related to digital electronic systems. The main objective for this course is the study of the basic techniques for the analysis and design of digital systems, setting up the basic knowledge and easing the study of complex systems to be covered in further courses.

This is a compulsory course taught in the third year of the Industrial Electronic Engineering degree during the first semester (autumn semester). This course has a length of 6 ECTS from which 3 ECTS are for theory classes, 1 ECTS for problem solving classes and 2 ECTS for laboratory sessions.

This course covers a global vision of digital systems inside the field of digital electronic systems. The proposed topics will allow the student to design a basic digital system and also analysing the requirements needed for implementing a digital design. In order to achieve these goals, the students will learn about different digital systems such as combinational and sequential subsystems, timing circuits, basic digital integrated circuits, programmable logic circuits, VHDL language, etc.

This is a practical course. The principles of digital design are accompanied with examples. Students will perform frequent exercises, both for analysis and design of digital systems which will further test and

create in the laboratory.

As a summary, this course provides a basic foundation for design and analysis of digital electronic systems and their associated circuits.

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PREVIOUS KNOWLEDGE

RELATIONSHIP TO OTHER SUBJECTS OF THE SAME DEGREE

There are no specified enrollment restrictions with other subjects of the curriculum.

OTHER REQUIREMENTS

In order to get the most out of the course, the student must have some previous knowledge and skills obtained in previous courses related to basic electronics. The main requirements are:

Measurement of electronic magnitudes as voltage and current
Use of electronic circuit simulators.
Being used to work in an electronics laboratory: usage of basic equipment, etc.
Logic families: bipolar and CMOS logic.

COMPETENCES / LEARNING OUTCOMES

1404 - Degree in Industrial Electronic Engineering

CE3 - Knowledge of the basics and applications of digital electronics and microprocessors.

CE6 - Ability to design analogue, digital and power electronic systems.

CG3 - Knowledge of basic and technological subjects that allows students to learn new methods and theories and provides them with versatility to adapt to new situations.

CG4 - Ability to solve problems with initiative, decision-making skills, creativity and critical reasoning and to communicate and transmit knowledge, abilities and skills in the field of industrial engineering (with specific industrial electronics technology).

DESCRIPTION OF CONTENTS

1. INTRODUCTION TO DIGITAL ELECTRONIC SYSTEMS

Systems: Analysis and Synthesis. Boolean algebra. Simplification of logic functions. Logic Families. Temporal parameters of logic circuits.

2. COMBINATIONAL CIRCUITS

Definition. Analysis and synthesis. Implementation with NAND and NOR gates. XOR and XNOR functions. Multilevel circuits: hazards.

3. INTRODUCTION TO HARDWARE DESCRIPTION LANGUAGES

Historical review. Basics. Data Types. Sequential and concurrent instruction. Subprograms. Test benches.

4. MSI CIRCUITS

Encoders and decoders. Code converters. Multiplexers and Demultiplexers. Comparator circuits. Arithmetic circuits. Arithmetic-Logic Units. VHDL description: decoders, multiplexers and arithmetic circuits. Exercises.

5. FLIP-FLOP CIRCUITS.

RS flip-flop: synchronous and asynchronous operation. JK flip-flop. Flip-flop D. Flip-flop T. VHDL description of the Flip-flops. Exercises.

6. INTRODUCTION TO SEQUENTIAL CIRCUITS

Definition. Shift registers. Asynchronous counters. Synchronous counters: introduction and design. Types of counters: up-down, ring, Johnson. Examples of circuits MSI. VHDL description of the counters. Exercises.

7. DIGITAL CIRCUITS AND CLOCK TIMING

Schmitt Trigger gates. Digital timer circuits.

8. STATE MACHINE DESIGN

Introduction: Moore and Mealy machines. Analysis of synchronous sequential circuits. Synthesis methodology. VHDL description of Moore machines. Exercises.

9. INTRODUCTION TO PROGRAMMABLE LOGIC

SPLD types: PROM, PAL, PLA, GAL. Design flow. Time Specification. Introduction to CPLDs. Introduction to FPGAs: Xilinx families.

WORKLOAD

PRESENCIAL ACTIVITIES

Activity	Hours
Theory	30,00
Laboratory	20,00
Classroom practices	10,00
Total hours	**60,00**

NON PRESENCIAL ACTIVITIES

Activity	Hours
Attendance at other activities	0,00
Individual or group project	10,00
Independent study and work	35,00
Preparation of lessons	25,00
Preparation for assessment activities	0,00
Resolution of case studies	20,00
Total hours	**90,00**

TEACHING METHODOLOGY

The course is organised around three kinds of attending classes: theory class, problem solving class and laboratory class. Office hours are used as additional attending tool for students. Concerning out-of-classroom activities, additional exercises must be solved, as well as report preparation.

In theory and problem-solving classes, traditional teaching method will be used. In theory sessions the teacher will explain the basic contents of the course using different teaching tools as slide presentation, together with other tools (CG3,CG4,CE3,CE6). Problem-solving classes will use two different models. First, the teacher will propose and solve different problems which are essential for proper understanding of digital systems from students, learning to follow a procedure and identify the required elements needed to adequately solve a problem (CG3,CG4,CE3,CE6). Second, the teacher will propose a problem and the students must solve the problem being distributed into groups, individually, or using other group working techniques and always under direct supervision of the teacher (CG4,CE6); once completed, the solutions will be collected by the teacher and corrected by the teacher or the students (depending on the case).

Students have a specific office-hour calendar where the teacher is available in his office for any concern related to the course (problem solving, theory doubts, report guidance, etc.). The attending hours will be detailed at the beginning of the academic year. Additionally, there exist a distance 'office-hours' program where questions can be solved using e-mail contact, and it is also promoted the use of the students' portal 'Aula Virtual' provided by the University of Valencia, where all the information related to the course is available online.

Laboratory sessions are organized according to three basic principles: design, mounting (real or virtual mounting) and testing/simulating an electronic digital system (CG3,CG4,CE3,CE6). The estimated duration for each laboratory session is 3 hours. The session will be carried out by groups of, at most, two persons. The student will get the laboratory activities' guide in advance so that previous preparation time is allowed. Once in the laboratory, there exists a direct supervision from the teacher. The student must assume the responsibility for all the stages in the proposal: design, mounting and testing. The final goal of the laboratory is to obtain a working system according to initial specifications. Finally, a lab report will be required from the teacher (CE6)

During the semester, it's possible to perform different works to be done as homework. The proposed works will be related to complete the knowledge of digital electronic systems such as the present state of digital systems, the market of digital electronics, future trends, etc. Groups of two or three persons will be formed and a final report must be presented by each group.

All of the described activities will be always using the support of 'Aula Virtual' as the most important source of information and communication for the student.

EVALUATION

Assessment of student learning will take place following two models:

a) By assessing the result of the continuous evaluation from the exams (theory, test and laboratory) plus the note of laboratory practices. To qualify for this type of evaluation, the student must have regularly attended classes and theoretical problems. To average the test scores of theory and laboratory will require

each of them to equal or exceed 4 The final grade is obtained from the following considerations:

- The theory mark will emerge as a result of carrying on the dates indicated in the official calendar of the written examination. It will consist of five questions of theoretical and practical problems and two (CG3,CG4,CE3,CE6). All questions will be related to the contents of the agenda, and with similar issues and problems done in class difficulty. This classification corresponds to 35% of the final grade.
- Upon completion of the course, a multiple-choice test that will count for 20% of the final grade will be made (CG3,CG4,CE3,CE6).
- The laboratory note arise as a result of the realization of an individual at the end of the semester, which will include a number of issues directly related to the practices during the course exam (CG3,CG4,CE3,CE6). It will consist of the design, assembly and / or simulation of some of the sections made by students throughout the laboratory sessions to which they had to attend. Demonstrated skill, proficiency in the use of laboratory equipment and design development throughout the session will be assessed. To be submitted to the above discussion, is a prerequisite to regularly attended practices (you can not miss more than 1 session). This note is equal to 25% of the final grade.
- In addition to this paper, the performance of the practice site was assessed using a few simple questions at the end of each session (CG3,CG4,CE3,CE6). This ongoing evaluation of the work done by students in all lab sessions valued skill, interest and results. This paper translates into 20% of the final grade for the course.
- The final grade for the course will come from the following expression:

Final Score = 0,35*Ex_Theory+0,25 * Ex_Lab+0,2*Eval_Lab + 0,2 * Ex_Test

b) From a second call in which the qualification of the theory and / or laboratory exam can be improved by conducting a test. The exam will be held on the official date and will consist of a theoretical first part, in which the student must demonstrate his knowledge of the concepts and relations seen in class and a second part that will consist of a laboratory examination (CG3, CG4, CE3 , CE6). In this, the student will have to design, assemble and / or simulate certain digital systems related to the contents of the syllabus and with similar difficulty to the questions and practices developed in the laboratory scripts (CG3, CG4, CE3, CE6). To average the notes of the theory and laboratory exams it will be necessary that each one of them equal or superior to 4. The final note of the subject will leave of the following expression:

Final Score = 0,55*Ex_Theory+0,25 * Ex_Lab+0,2*Eval_Lab

Students who opt for option a), and who do not approve the subject in this way, may submit to the official examination in second call (modality b).

In any case, the evaluation system will be governed by what is established in the Evaluation and Qualification Regulations of the Universitat de València for Degrees and Masters (https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639).

Copying or plagiarism of any activity that is part of the evaluation will result in the impossibility of passing the course, and the student will then be subject to the appropriate disciplinary procedures indicated in the ACTION PROTOCOL FOR FRAUDULENT PRACTICES AT THE UNIVERSITY OF VALENCIA (ACGUV 123/2020).

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