

## PRÁCTICA 2. Programación de un sumador-restador de 3 bits.

### 1. Introducción.

Para la realización de cálculos binarios, es imprescindible la utilización de elementos capaces de realizar operaciones matemáticas. Las unidades aritmético-lógicas (ALU) contienen esencialmente capacidades aritméticas de suma y multiplicación. En esta práctica se desea diseñar un módulo sumador-restador de 3 bits sin signo de acarreo encadenado basado en un sumador de un bit con acarreo de entrada y salida. Este sumador de un bit se puede enlazar de modo que se puede construir un sumador de tantos bits como se desee de forma rápida y sencilla. La estructura de nivel superior de este sumador es la que se muestra en la figura siguiente

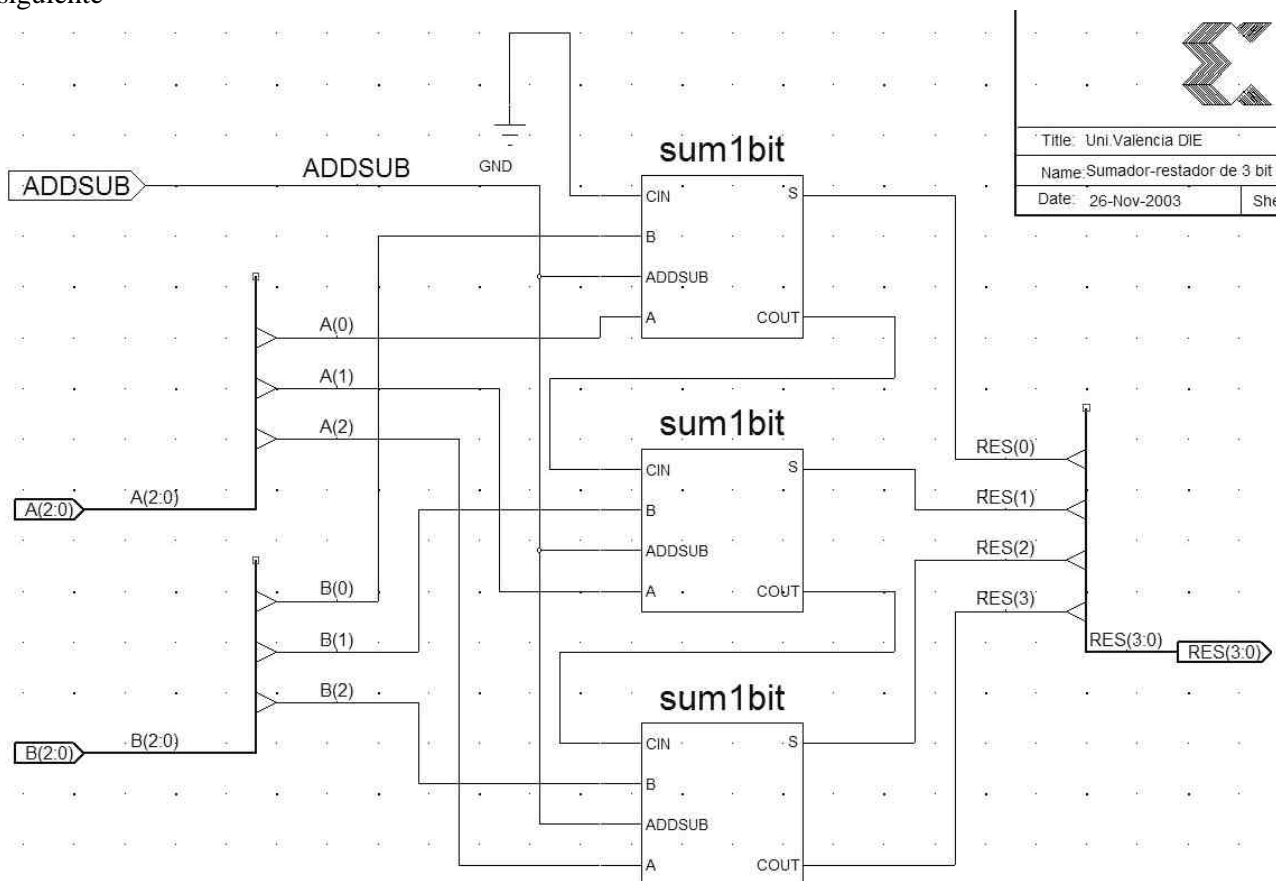


Figura 1. Esquema de un sumador-restador de 3 bits.

Cada módulo de 1 bit posee cuatro entradas (A, B, CIN y ADDSUB) y dos salidas (S, COUT). La entrada ADDSUB controla el resultado de la salida, efectuando la suma si su nivel lógico es '1', y la resta si su nivel lógico es '0', en cualquier caso, la operación se realiza entre los operandos A, B y CIN. Como ejemplo de funcionamiento, si  $A=3$ ,  $B=6$ , el resultado de la suma es 9, y dado que la resta siempre se realiza como  $A-B$ , el resultado es:  $D=13$ . Un ejemplo de simulación es:



Figura 2. Simulación de las operaciones del sumador-restador de 3 bits.

### 2. Objetivo de la práctica.

En esta práctica vamos a realizar la implementación sobre un dispositivo lógico programable, en este caso sobre una FPGA Xilinx de la familia VirtexE modelo XCV100EPQ240-6. Los pasos a realizar son:

1. Diseño del módulo sumador-restador de un bit.
2. Simulación del módulo sumador-restador de un bit.
3. Creación de un elemento de librería para obtener un símbolo capaz de ser utilizado como un elemento más.
4. Simulación funcional del módulo de 3 bits, probando los diversos modos de operación, es decir, en modo suma, en modo resta, y con varias combinaciones de entrada para A y B.
5. Generación de un módulo de nivel superior donde se realice una decodificación de las salidas para ser mostradas en un display de 7 segmentos, en este nivel también se incluirá una señal de entrada que permita visualizar un nuevo resultado de la suma de los elementos de entrada cada vez que ocurre el paso de estado bajo a alto para esta entrada. Se incluye una entrada de reset por la que cuando se activa, la salida toma un valor cero.
6. Simular el sistema total.

El aspecto del dispositivo a nivel de entradas y salidas externas es el siguiente:

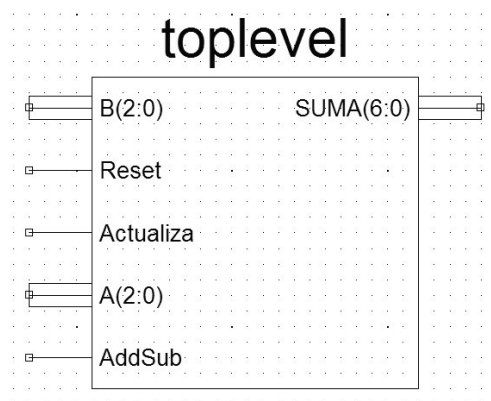


Figura 3. Símbolo completo con entradas y salidas del sistema final a diseñar.

## 4. Diseño y simulación.

Primeramente se debe diseñar el sumador-restador de un bit, una vez simulado, se genera un elemento de librería para el mismo. A continuación se diseña el sistema sumador-restador de 3 bit empleando el símbolo de librería que se acaba de crear. Una vez diseñado y simulado correctamente se genera otro símbolo de librería para el módulo de 3 bits. Como se desea visualizar el resultado en un display de 7 segmentos, se debe incluir en el proyecto el fichero *hex2led.vhd* proporcionado. Para este fichero VHDL, también se genera el símbolo esquemático. En nuevo esquema se incluye el módulo de 3 bits, el decodificador a 7 segmentos y la lógica necesaria para hacer que el sistema sólo actualice el cálculo cuando se le proporcione la orden desde la entrada "Actualiza". Se simula el sistema completo y se comprueba que funciona correctamente.

**NOTA:** Si se necesita poner señales de entrada a nivel lógico cero ó uno, en la librería de símbolos se dispone de los símbolos GND y VCC respectivamente.

## 5. Implementación.

Una vez simulado, para que el diseño disponga de las entradas y salidas que corresponden a la ubicación de los interruptores y LED que existen en la placa, es necesario conocer el número de patilla donde cada uno se ubica. En los anexos a esta memoria se muestran unos esquemas y una descripción de la placa donde, junto con la exploración física de la placa disponible en el laboratorio, debéis ser capaces de encontrar el número de patilla que demos asignar a cada entrada y salida del diseño.

Escribe a continuación la asignación de cada patilla:

```
NET "suma<6>"      LOC = ;
NET "suma<5>"      LOC = ;
NET "suma<4>"      LOC = ;
NET "suma<3>"      LOC = ;
```

```

NET "suma<2>"          LOC = ;
NET "suma<1>"          LOC = ;
NET "suma<0>"          LOC = ;
NET "reset"            LOC = ;
NET "a<2>"             LOC = ;
NET "a<1>"             LOC = ;
NET "a<0>"             LOC = ;
NET "addsub"           LOC = ;
NET "actualiza"        LOC = ;
NET "b<2>"             LOC = ;
NET "b<1>"             LOC = ;
NET "b<0>"             LOC = ;
    
```

Para realizar la asignación de patillas es necesario que en la ventana de fuentes añadamos una nueva fuente (*New Source*), en este caso del tipo *User Constraint File*. Una vez creada, aparece un fichero con extensión *.ucf*, que teniéndolo seleccionado ejecutaremos la opción de la ventana de procesos llamada *User Constraints -> Assign Package Pins*. Esta opción nos abre el editor PACE, donde tenemos las entradas y salidas que podemos llevar a la patilla a asignar.

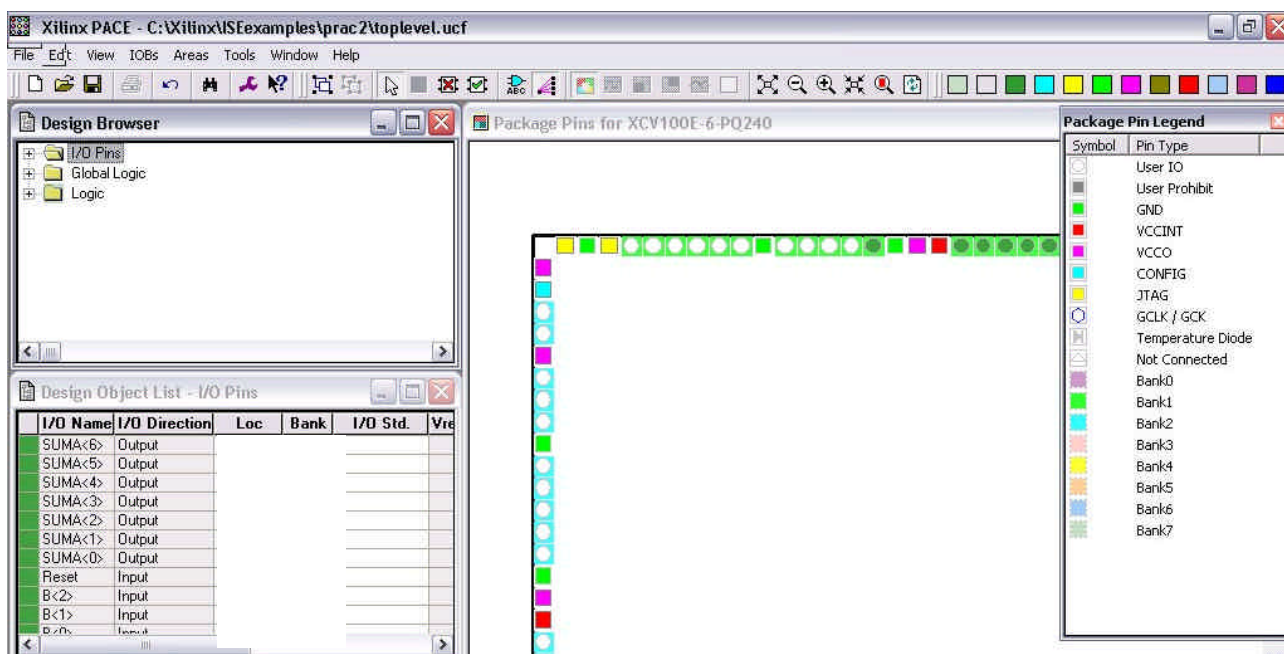


Figura 4. Imagen de PACE, editor de restricciones, empleado en este caso para asignar patillas en el dispositivo FPGA a emplear.

Una vez realizada la asignación de patillas ya podremos proceder a la implementación del sistema. Para ello, ejecutaremos la opción *Implement Design* que automáticamente realizará el proceso de asignar los recursos lógicos. Si el proceso finaliza correctamente, visualizar los informes y buscar la información que se solicita a continuación:

```

Number of Slices:      ..... out of 1,200
Number of 4 input LUTs: ..... out of 2,400
Number of bonded IOBs: ..... out of 158
IOB Flip Flops:      .....
    
```

## 6. Programación de la placa.

Para generar el fichero que sirve para descargar el programa en la placa se ejecuta la acción *Generate Programming File*.

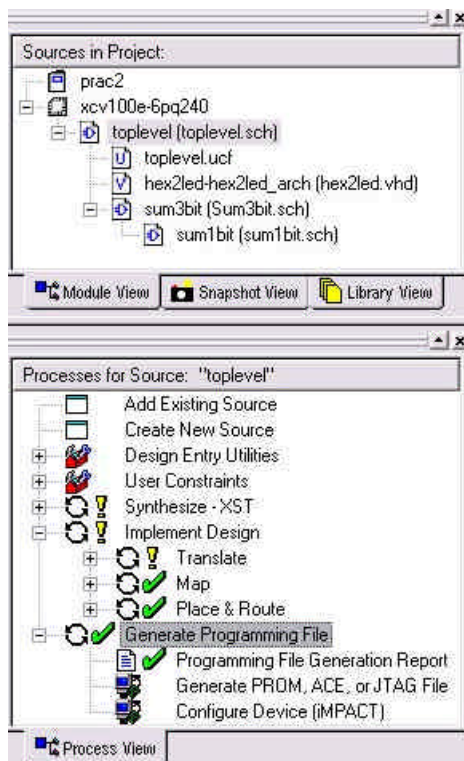


Figura 5. Ventanas de fuentes y procesos para el diseño de esta sesión.

Una vez finalizado el proceso estaremos en disposición de encender la fuente de alimentación de la placa para posteriormente entrar dentro del programa iMPACT que es el encargado de configurar el proceso de programación.

Al arrancar este programa aparece un asistente que solicita información acerca del tipo de programación que se desea realizar. Las opciones que se deben elegir son:

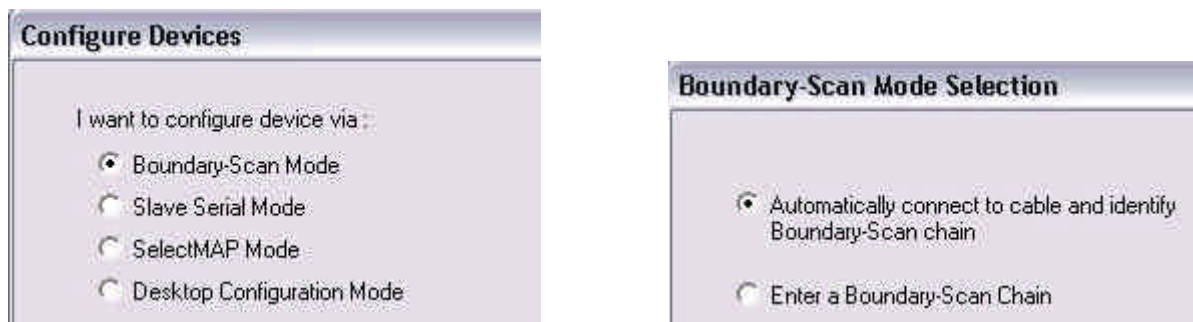


Figura 6. Opciones a seleccionar en iMPACT para programar el dispositivo.

El proceso de reconocimiento automático debe reconocer dos dispositivos de programación, una memoria EEPROM XC18v01 que no vamos a emplear y la FPGA, para ello, nos pedirá el fichero de programación de cada dispositivo, para el caso de la memoria, le decimos que lo ignore (Bypass), y para el caso de la FPGA procederemos a indicarle el fichero *.bit* que se nos ha generado en la carpeta de nuestro proyecto.

Finalmente, el aspecto de iMPACT es el que sigue:

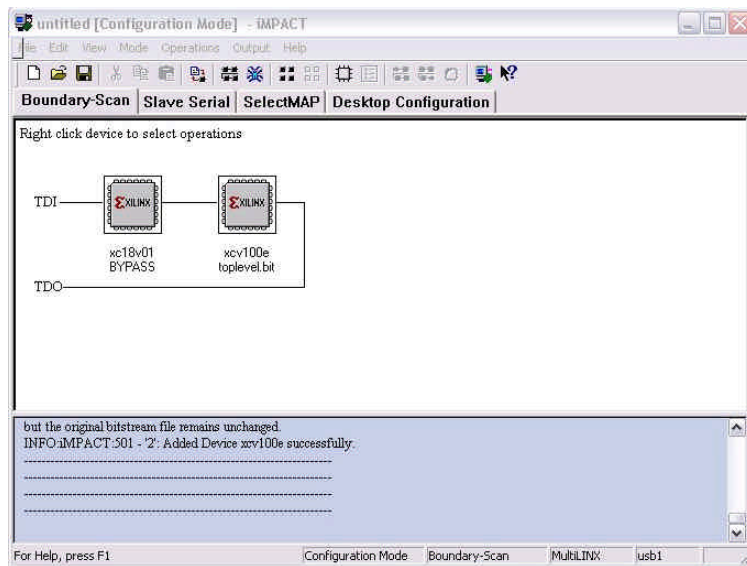


Figura 7. Ventana principal de IMPACT.

Se selecciona la FPGA (se selecciona en un color verde), y se ejecuta la opción **Operations -> Program**, procediendo a la verificación de la misma.

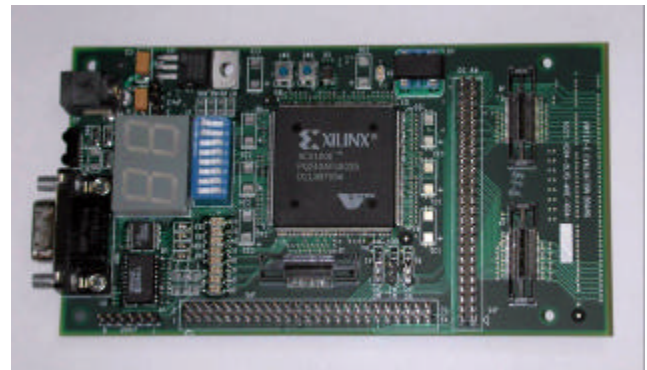
## Features

- FPGA  
Xilinx® Virtex-E XCV100E-6PQ240C
- SPROM  
Xilinx® XC18V01SO20C
- Board I/O Connectors  
Two 50-pin, 0.1 Header connector  
Pads for three MICTOR connectors  
Pads for one 140 pin General Purpose I/O interface
- Power  
+5.0 Power Connector  
+3.3 V Regulated Supply  
+1.8 V Regulated Supply  
Full Bypass Capacitance
- Communication  
RS232 Serial Port
- Configuration  
JTAG Header Connector  
In-System Programmable PROM  
JTAG Download Cable
- Miscellaneous  
8 DIP switches  
2 Push-buttons,  
Dual Digit 7 Segment LED, right hand decimal  
Infrared Transceiver  
8 LEDs  
40 MHz Oscillator  
Digital Thermometer
- Demonstration application (Source VHDL)  
Simple RS232  
Digital Thermometer  
LED Patterns

## Description

The Evaluation Virtex-E Kit is used by engineers as a platform to test FPGA designs that are targeted to the Xilinx Virtex-E device. It is also a great tool for beginners to get aquatinted with FPGAs and VHDL.

The Virtex-E device is located in the center of the board. It can be configured via a JTAG download or from the on board configuration PROM. The configuration PROM is also programmable through the JTAG cable. Over 85 IO signals are connected from the FPGA to 0.1 header connectors for user connections. Other IO are connected to 8 LED, 8 dip switches, Two push buttons, RS-232 line driver/receiver, and a digital thermometer.



## Demo Application.

The board is supplied with complete VHDL source code that:

- 1) Sequences LEDs
- 2) Reads Dip Switches/push buttons
- 3) Senses Temperature and displays value on dual 7 segment LED
- 4) Transmits startup message through RS-232 connector.
- 5) Echoes RS-232 commands. (Serial cable not included)

## Ordering Information

The following table lists the development system part numbers and available software options.

Internet Link at <http://www.em.avnet.com/>.

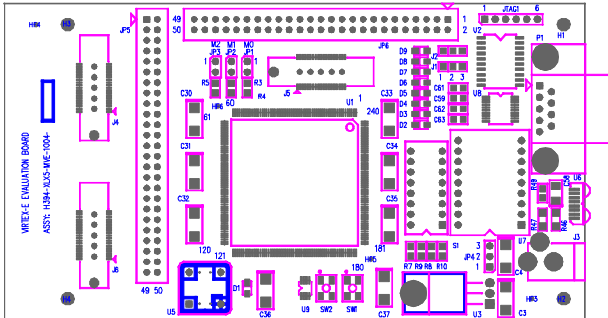
**Table 1 Evaluation Virtex-E Board**

Part Number	Hardware
ADS-XLX-VE-EVL	Xilinx Virtex-E Evaluation Kit



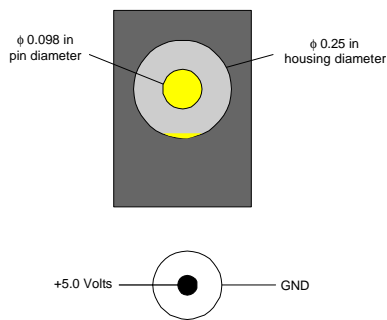
## ADS Evaluation Virtex-E Board

This section provides information basic to the design of Evaluation Virtex-E Board board.



### Power

The majority of the design is powered at 3.3V with the Virtex-E FPGA core powered at 1.8V. The board should be powered by a 5-volt bench supply. The 3.3V is derived via a linear regulator. A linear regulator from the 3.3V provides the 1.8V Xilinx core voltage. A barrel connector J3 (RAPC712) is provided on the board for lab supply connections. The center tap is +5.0 volts and the outer is GND. Note: The lab supply should be regulated at 5.0 volts. While current requirements are dependent on the user application, it is suggested to limit your supply to 1.5 amps on initial power up.



### Printed Circuit Board

The Evaluation Virtex-E Board printed circuit board is an 6-layer board with four signal layers, a full 3.3V power plane incorporating an isolated 1.8V mini-plane, and full ground plane. The board stack-up layers 1 through 6 is:

- 1) "Component side"/signal
- 2) Ground Plane
- 3) Signal
- 4) Signal
- 5) Power: 3.3V and 1.8V
- 6) "Solder side"/signal

### Virtex-E FPGA

The Virtex-E Field-Programmable Gate Array device (U1) utilized in this design is the 100+K-system gate device (XCV100E) in a PQ240 package.

### FPGA Configuration

Configuration information is provided from two sources; the JTAG Connector (JTAG0), and configuration PROM.

**Table 2 JTAG Connector**

Signal Name	JTAG Connector Pin #
VCC	1
TDI	2
TMS	3
TCK	4
TDO	5
GND	6

Jumpers JP1, JP2 and JP3 select the configuration mode of the Virtex. The following table shows the jumper setting needed for each mode.

**Table 3 Mode Select**

Configuration Mode	Pull-ups	JP3/M2	JP2/M1	JP1/M0
Master-serial	No	OFF /LOW	OFF /LOW	OFF /LOW
Boundary-scan	No	ON /HIGH	OFF /LOW	ON /HIGH
SelectMAP	No	ON /HIGH	ON /HIGH	OFF /LOW
Slave-serial	No	ON /HIGH	ON /HIGH	ON /HIGH
Master-serial	Yes	ON /HIGH	OFF /LOW	OFF /LOW
Boundary-scan	Yes	OFF /LOW	OFF /LOW	ON /HIGH
SelectMAP	Yes	OFF /LOW	ON /HIGH	OFF /LOW
Slave-serial	Yes	OFF /LOW	ON /HIGH	ON /HIGH

The LED D1 indicates the output level of the DONE pin of the Virtex-E device. It will illuminate when the Virtex-E configuration is complete.

### System Clock

An oscillator socket clock output is connected to the Virtex-E device. U5 is connected to Global Clock Input #0 (PQ240 pin #P92), The U5 socket is populated with a 40 MHz oscillator.

### Asynchronous (RS232) Communication Interface

The ADM3222 device provides level translation for a single RS232 interface (DB9 connector). The second translation port on the device is terminated and unused.

**Table 4 RS232 Interface Signals**

RS232 SIGNAL	Virtex-E PIN #
R1OUT	P216
T1IN	P217
EN_N	P218
SD_N	P219

**Table 5 RS232 Connector Pinout**

Signal Name	P2 (DB9) connector Pin #
TX out	2
RX in	3
GND	5

## Miscellaneous

The “Miscellaneous” interfaces on the Virtex-E board consist of a single 8-position DIP switch (8-individual SPST switches), 8 LEDs, and two push-button switches.

**Table 6 Dip Switch Signals**

DIP SW	Virtex-E PIN #
#1	P194
#2	P195
#3	P199
#4	P200
#5	P201
#6	P202
#7	P203
#8	P205

**Table 7 Push Button Switch Signals**

BUTTON	Virtex-E PIN #
SW1	P206
SW2	P208

**Table 8 LED Control Signals**

LED	Virtex-E PIN #
D2	P27
D3	P28
D4	P3
D5	P4
D6	P5
D7	P6
D8	P7
D9	P9

**Table 9 Dual Segmented LED Signals**

LED	Virtex-E PIN #
A1	P221
B1	P222
C1	P223
D1	P224
E1	P228
F1	P229
G1	P230
Dp1	P231
A2	P234
B2	P235
C2	P236
D2	P237
E2	P238
F2	P186
G2	P187
Dp2	P188

**Table 10 Infrared Signals**

LED	Virtex-E PIN #
TXD	P102
RXD	P101
SHDN	P100

**Table 11 Digital Thermometer**

LED	Virtex-E PIN #
CE	P160
SCLK	P159
SDI	P161
SDO	P162



## I/O Signal Headers

Two 50-pin connectors provides 84 Virtex-E I/O lines and 6 ground pins.

**Table 12 GPIO Signals JP5**

GPIO CONNECTOR PIN #	Virtex-E PIN #
1	P86
2	P84
3	P82
4	P81
5	P80
6	P79
7	P78
8	P74
9	P73
10	P72
11	P71
12	P70
13	P68
14	P67
15	P66
16	P65
17	P64
18	P63
19	P99
20	P97
21	P96
22	P95
23	P94
24	P118
25	P117
26	P115
27	P114
28	P113
29	P111
30	P110
31	P109
32	P108
33	P149
34	P147
35	P144
36	P142
37	P141
38	P140
39	P134
40	P133
41	P132
42	P131
43	P130
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	GND
49	GND
50	GND

**Table 13 GPIO Signals JP6**

GPIO CONNECTOR PIN #	Virtex-E PIN #
1	P31
2	P33
3	P34
4	P35
5	P36
6	P38
7	P39
8	P40
9	P41
10	P42
11	P46
12	P47
13	P48
14	P49
15	P50
16	P52
17	P53
18	P54
19	P56
20	P57
21	P10
22	P11
23	P12
24	P13
25	P17
26	P18
27	P19
28	P20
29	P21
30	P23
31	P24
32	P26
33	P128
34	P127
35	P126
36	P125
37	P175
38	P174
39	P173
40	P171
41	P170
42	P169
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	GND
49	GND
50	GND

## Logic Analyzer Connector

Three AMP™ MICTOR connector pads are provided to connect to a logic analyzer's mass termination cable.

**Table 14 MICTOR J4**

Connector PIN #	Virtex-E PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P210*	CLK_OUT
6	P92	OSC
7	P108	ADDRESS31
8	P65	ADDRESS15
9	P109	ADDRESS30
10	P66	ADDRESS14
11	P110	ADDRESS29
12	P67	ADDRESS13
13	P111	ADDRESS28
14	P68	ADDRESS12
15	P113	ADDRESS27
16	P70	ADDRESS11
17	P114	ADDRESS26
18	P71	ADDRESS10
19	P115	ADDRESS25
20	P72	ADDRESS9
21	P117	ADDRESS24
22	P73	ADDRESS8
23	P118	ADDRESS23
24	P74	ADDRESS7
25	P94	ADDRESS22
26	P78	ADDRESS6
27	P95	ADDRESS21
28	P79	ADDRESS5
29	P96	ADDRESS20
30	P80	ADDRESS4
31	P97	ADDRESS19
32	P81	ADDRESS3
33	P99	ADDRESS18
34	P82	ADDRESS2
35	P63	ADDRESS17
36	P84	ADDRESS1
37	P64	ADDRESS16
38	P86	ADDRESS0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

**Table 15 MICTOR J5**

Connector PIN #	Virtex-E PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P213*	GCK3
6	P89*	GCLK1
7	P26	DATA31
8	P52	DATA15
9	P24	DATA30
10	P50	DATA14
11	P23	DATA29
12	P49	DATA13
13	P21	DATA28
14	P48	DATA12
15	P20	DATA27
16	P47	DATA11
17	P19	DATA26
18	P46	DATA10
19	P18	DATA25
20	P42	DATA9
21	P17	DATA24
22	P41	DATA8
23	P13	DATA23
24	P40	DATA7
25	P12	DATA22
26	P39	DATA6
27	P11	DATA21
28	P38	DATA5
29	P10	DATA20
30	P36	DATA4
31	P57	DATA19
32	P35	DATA3
33	P56	DATA18
34	P34	DATA2
35	P54	DATA17
36	P33	DATA1
37	P53	DATA16
38	P31	DATA0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

Table 16 MICTOR J6

Connector PIN #	Virtex-E PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P210*	CLK_OUT
6	P191*	CLK_IN
7	P178	DOUT
8	P175	CNTL15
9	P208	SWITCH9
10	P125	CNTL14
11	P206	SWITCH8
12	P126	CNTL13
13	P162	TEMP_SDO
14	P127	CNTL12
15	P161	TEMP_SDI
16	P128	CNTL11
17	P160	TEMP_CE
18	P130	CNTL10
19	P159	TEMP_SCLK
20	P131	CNTL9
21	P220	RS232SD_N
22	P132	CNTL8
23	P218	RS232EN_N
24	P133	CNTL7
25	P217	RS232TX
26	P139	CNTL6
27	P216	RS232RX
28	P140	CNTL5
29	P169	CNTL20
30	P141	CNTL4
31	P170	CNTL19
32	P142	CNTL3
33	P171	CNTL18
34	P144	CNTL2
35	P173	CNTL17
36	P147	CNTL1
37	P174	CNTL16
38	P149	CNTL0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

\*Note: A zero ohm resistor may be required to access the noted signals.

### AvBus Connector

High-density connector pads are located on bottom of the board. The signals are listed in the following table.

Table 17 AvBus Connector P2

Name	FPGA PIN #	Connector PIN #	FPGA PIN #	Name
ADDRESS0	P86	71	1	N/C
GND	GND	72	2	P84
ADDRESS3	P81	73	3	P82
ADDRESS4	P80	74	4	GND
GND	GND	75	5	P79
ADDRESS7	P74	76	6	P78
ADDRESS8	P73	77	7	GND
AUX_+3.3V	+3.3V	78	8	P72
ADDRESS11	P70	79	9	P71
ADDRESS12	P68	80	10	GND
GND	GND	81	11	P67
ADDRESS15	P65	82	12	P66
ADDRESS16	P64	83	13	N/C
GND	GND	84	14	P63
ADDRESS19	P97	85	15	P99
ADDRESS20	P96	86	16	GND
GND	GND	87	17	P95
ADDRESS23	P118	88	18	P94
ADDRESS24	P117	89	19	GND
AUX_+3.3V	+3.3V	90	20	P115
ADDRESS27	P113	91	21	P114
ADDRESS28	P111	92	22	GND
GND	GND	93	23	P110
ADDRESS31	P108	94	24	P109
DATA0	P31	95	25	N/C
GND	GND	96	26	P33
DATA3	P35	97	27	P34
DATA4	P36	98	28	GND
GND	GND	99	29	P38
DATA7	P40	100	30	P39
DATA8	P41	101	31	GND
AUX_+3.3V	+3.3V	102	32	P42
DATA11	P47	103	33	P46
DATA12	P48	104	34	GND
GND	GND	105	35	P49
DATA15	P52	106	36	P50
DATA16	P53	107	37	N/C
GND	GND	108	38	P54
DATA19	P57	109	39	P56
DATA20	P10	110	40	GND
GND	GND	111	41	P11
DATA23	P13	112	42	P12
DATA24	P17	113	43	GND
AUX_+3.3V	+3.3V	114	44	P18
DATA27	P20	115	45	P19
DATA28	P21	116	46	GND
GND	GND	117	47	P23
DATA31	P26	118	48	P24
CNTL0	P149	119	49	N/C
GND	GND	120	50	P147
CNTL3	P142	121	51	P144
CNTL4	P141	122	52	GND
GND	GND	123	53	P140
CNTL7	P133	124	54	P139
CNTL8	P132	125	55	GND
AUX_+3.3V	+3.3V	126	56	P131
CNTL11	P128	127	57	P130

Name	FPGA PIN #	Connector	PIN #	FPGA PIN #	Name
CNTL12	P127	128	58	GND	GND
GND	GND	129	59	P126	CNTL13
CNTL15	P175	130	60	P125	CNTL14
CNTL16	P174	131	61	N/C	N/C
GND	GND	132	62	P173	CNTL17
CNTL19	P170	133	63	P171	CNTL18
CNTL20	P169	134	64	GND	GND
GND	GND	135	65	P191*	CLK_IN
CLK_OUT	P210*	136	66	P210*	CLK_OUT_FB
TMS	⊕	137	67	GND	GND
AUX_+3.3V	+3.3V	138	68	⊕	TDO
TDI	⊕	139	69	⊕	TCK
TRS	⊕	140	70	GND	GND

\*Note: A zero ohm resistor may be required to access the noted signals.

⊕Note: Reference Schematic for current JTAG signal paths.

## Demonstration Program

Supplied with the development system is a demonstration program file that utilizes several devices on the evaluation board. The demonstration program uses the evaluation development board as a standalone platform that is connected to a lab supply and a terminal emulation program. On power up the onboard PROM will configure the FPGA. Upon completion of the configuration the FPGA functionality and input/output signal will activate. A start up serial message will be sent to the terminal port via the RS-232 connection. The LEDs will display a back and forth scanning pattern or 8-bit value corresponding to the current temperature. The Dual segmented display will count up or display the current temperature.

### Additional Items Needed:

- Lab power supply, 5.0 volts at 1.5 amps.
- Serial Terminal or Terminal Emulator.
- RS-232 cable

### Setup:

- 1) Attach the lab supply to the power connector on the Evaluation Board.
- 2) Attach the serial terminal to the P1 connector of the Evaluation Board.
- 3) Set the Serial Terminal to: 8 data bits, 1 stop, No parity, 9600 baud.
- 4) Verify jumper are NOT installed on JP1, JP2, and JP3.
- 5) Verify JP4 is installed across pins 1 and 2.

### Power UP:

- 6) Apply power to the Evaluation Board.
- 7) The DONE LED D1 will light on the completion of the download.

### Reset:

- 8) Press the Soft Reset button SW1 to reset the board.

### Serial Demo

- 9) Press the button SW2 to send the startup message.
- 10) The Power up message is displayed on the serial terminal.
- 11) All characters typed should be echoed to the terminal.
- 12) Press the Reset button again to "reset" startup message.

### LED SCAN

- 13) Set the dipswitch S1 dip 1 to ON (rocker up).
- 14) The LEDs should be blinking such that the illuminated led should be scanning back and forth through the LED array.

### UP COUNTER

- 15) Set the dipswitch S1 dip 2 to ON (rocker down).
- 16) The Dual segmented LEDs should be counting up.

### TEMPERATURE

- 17) Set the dipswitch S1 dip 1 to OFF (rocker down).
- 18) The LED should now display the temperature in °C in two's complement binary. See the following table.
- 19) Set the dipswitch S1 dip 2 to OFF (rocker down).
- 20) The Dual segmented LEDs should now display the temperature in °C.
- 21) Hold your finger on U5 to change the temperature.

LED Pattern (D9..D2)	Decimal Value (°C)
0111 1000	+120C
0001 1001	+25C
0000 1010	+10C
0000 0000	0C
1111 0101	-10C
1110 0110	-25C
1100 1001	-55C

## Relevant Documents

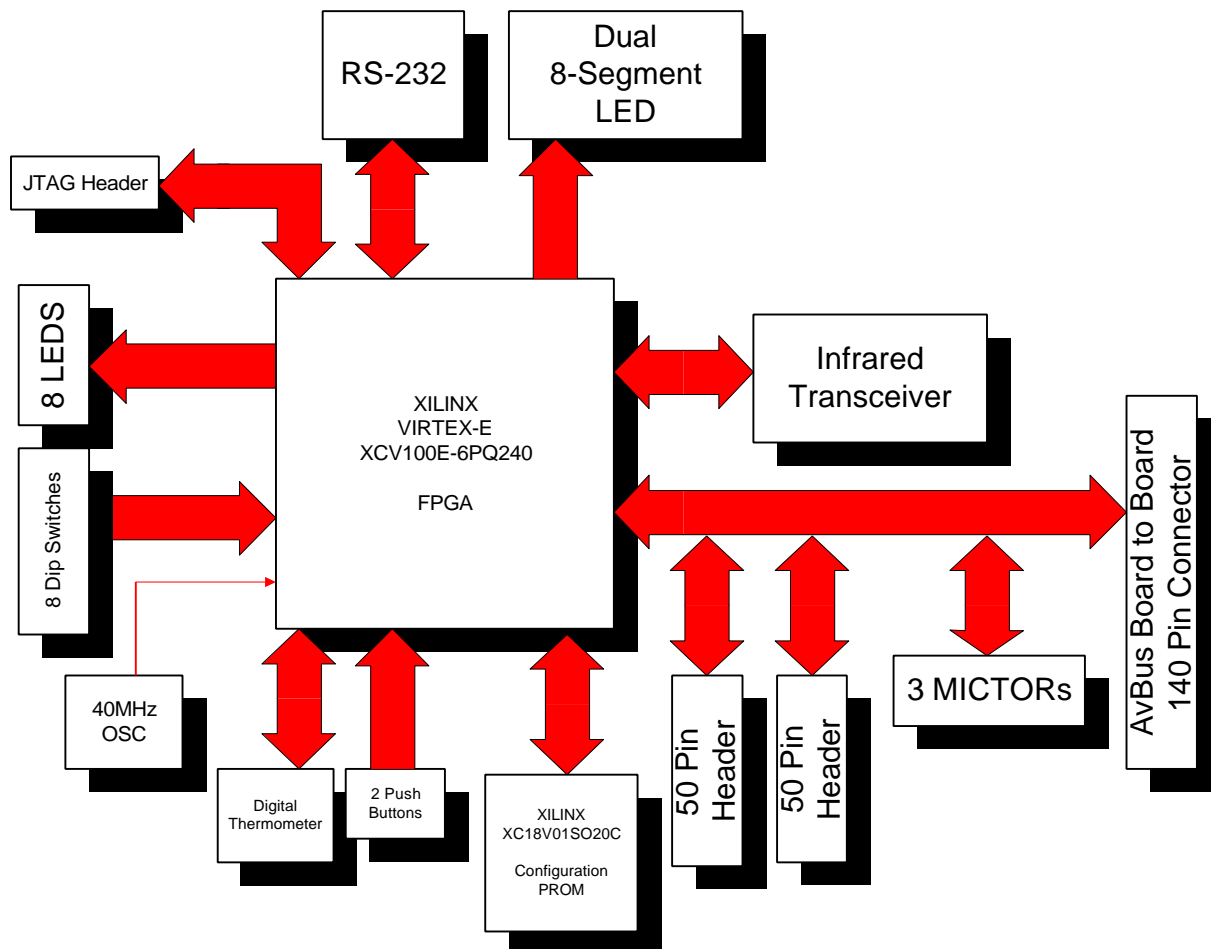
Documents relevant to this application are listed in the following table.

**Table 18. Relevant Documents and Links**

Document	Source
XILINX XC18V01 Configuration PROM Data Sheet	<a href="http://www.xilinx.com/partinfo/ds026.pdf">http://www.xilinx.com/partinfo/ds026.pdf</a>
Analog Devices ADM3222 3V RS232 Line Driver/Receiver Data Sheet	<a href="http://www.analog.com/pdf/ADM3202_0.pdf">http://www.analog.com/pdf/ADM3202_0.pdf</a>

Document	Source
XILINX VIRTEX-E FPGA Data Sheet	<a href="http://www.xilinx.com/partinfo/ds022.pdf">http://www.xilinx.com/partinfo/ds022.pdf</a>

## Block Diagram

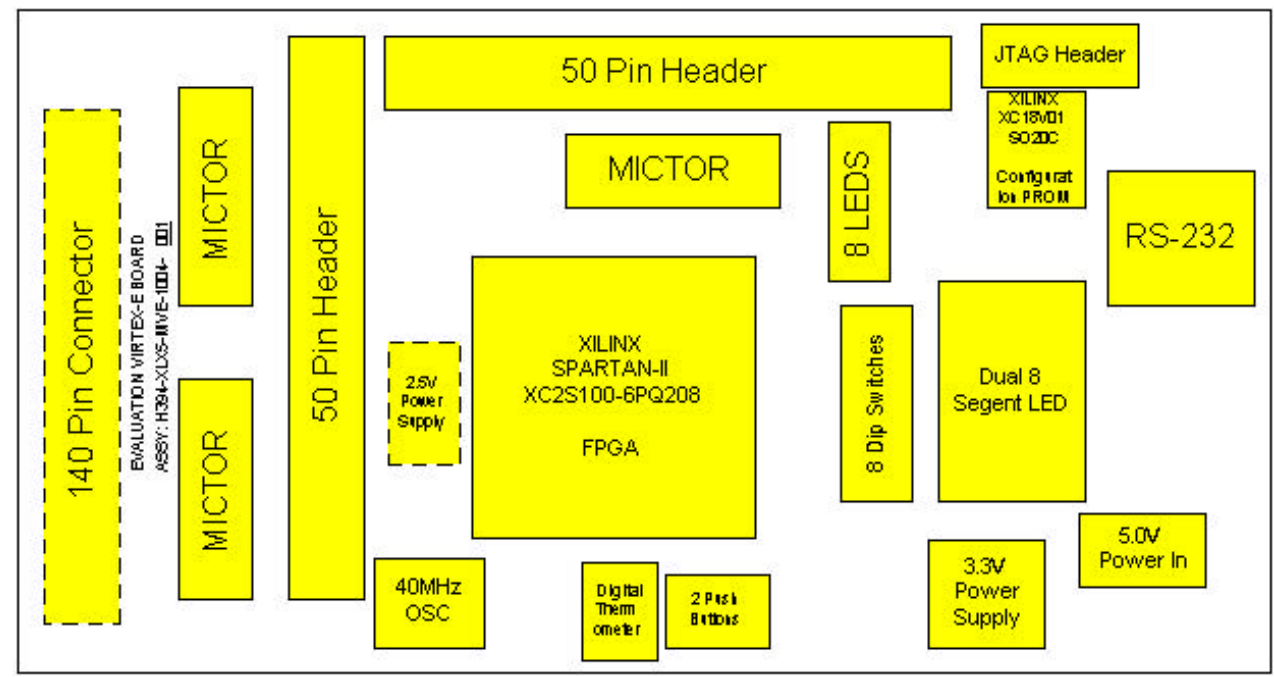
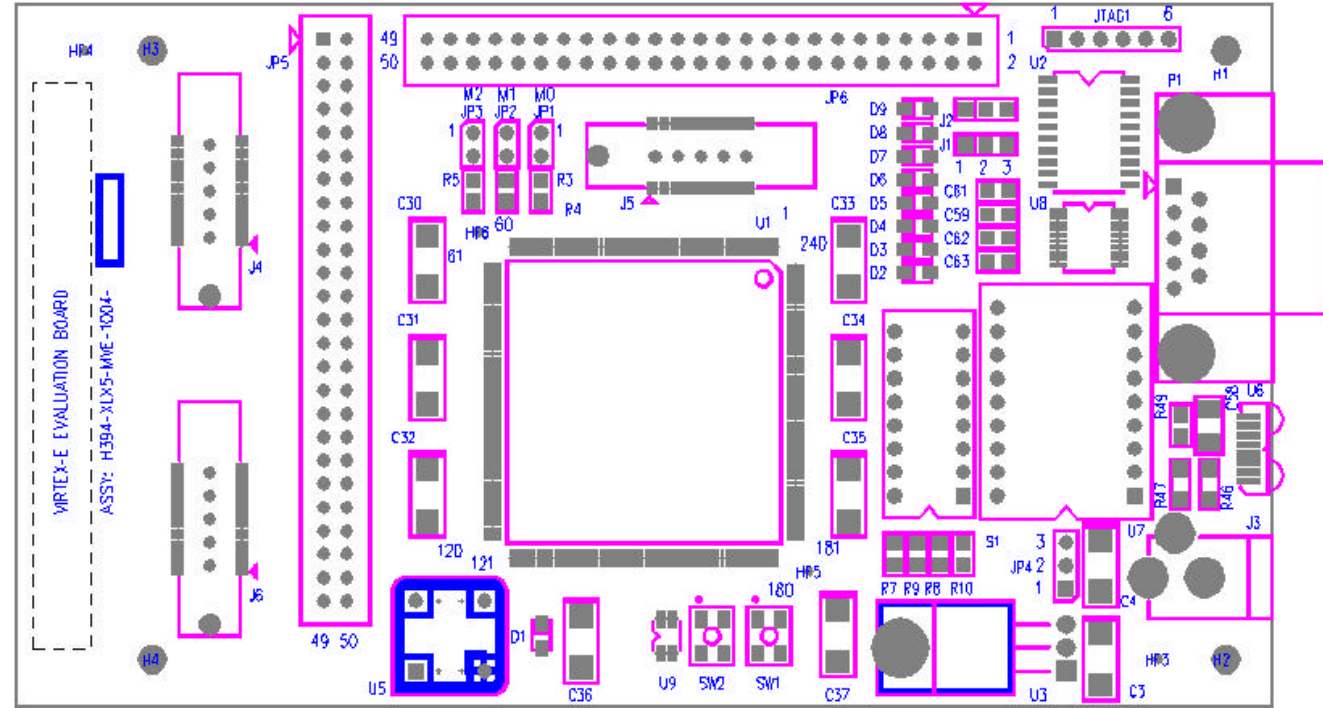


## Revisions

Version 1.0	Initial Release.
Version 1.1	Fixed typographical errors.

Mini-Virtex-E Evaluation Board	
Avnet Design Services	
www.em.avnet.com	
Function	Sheet Number
Lead Sheet	1
FPGA, SPROM	2
Power	3
Mictor and Header Connectors	4
Switch, LED, OSC	5
Daughter Board Connector	6

REV	SHEET	DESCRIPTION	DATE
A	ALL	Initial Release	11-OCT-2000



Copyright 2000, Avnet, Inc. All Rights Reserved.

This material may not be reproduced, distributed, republished, displayed, posted, transmitted or copied in any form or by any means without the prior written permission of Avnet, Inc. AVNET and the AV logo are registered trademarks of Avnet, Inc. All trademarks and trade names are the properties of their respective owners and Avnet, Inc disclaims any proprietary interest or right in trademarks, service marks and trade names other than its own.

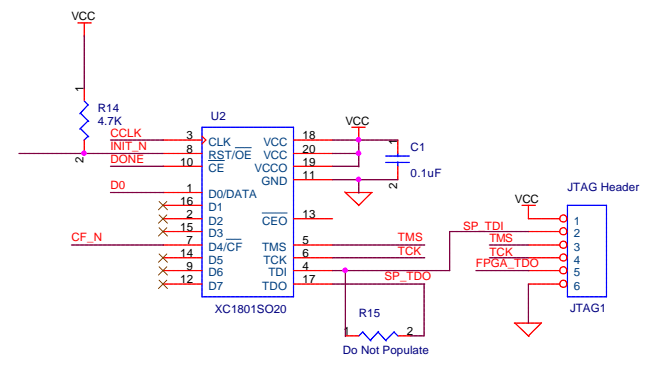
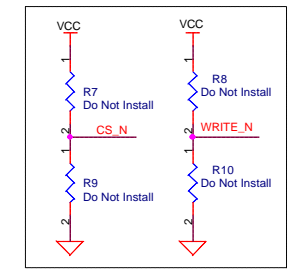
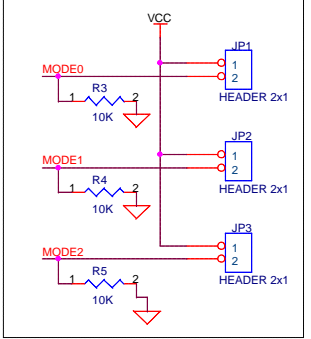
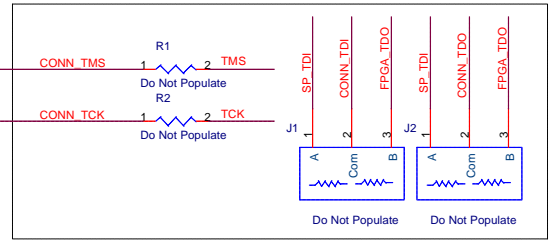
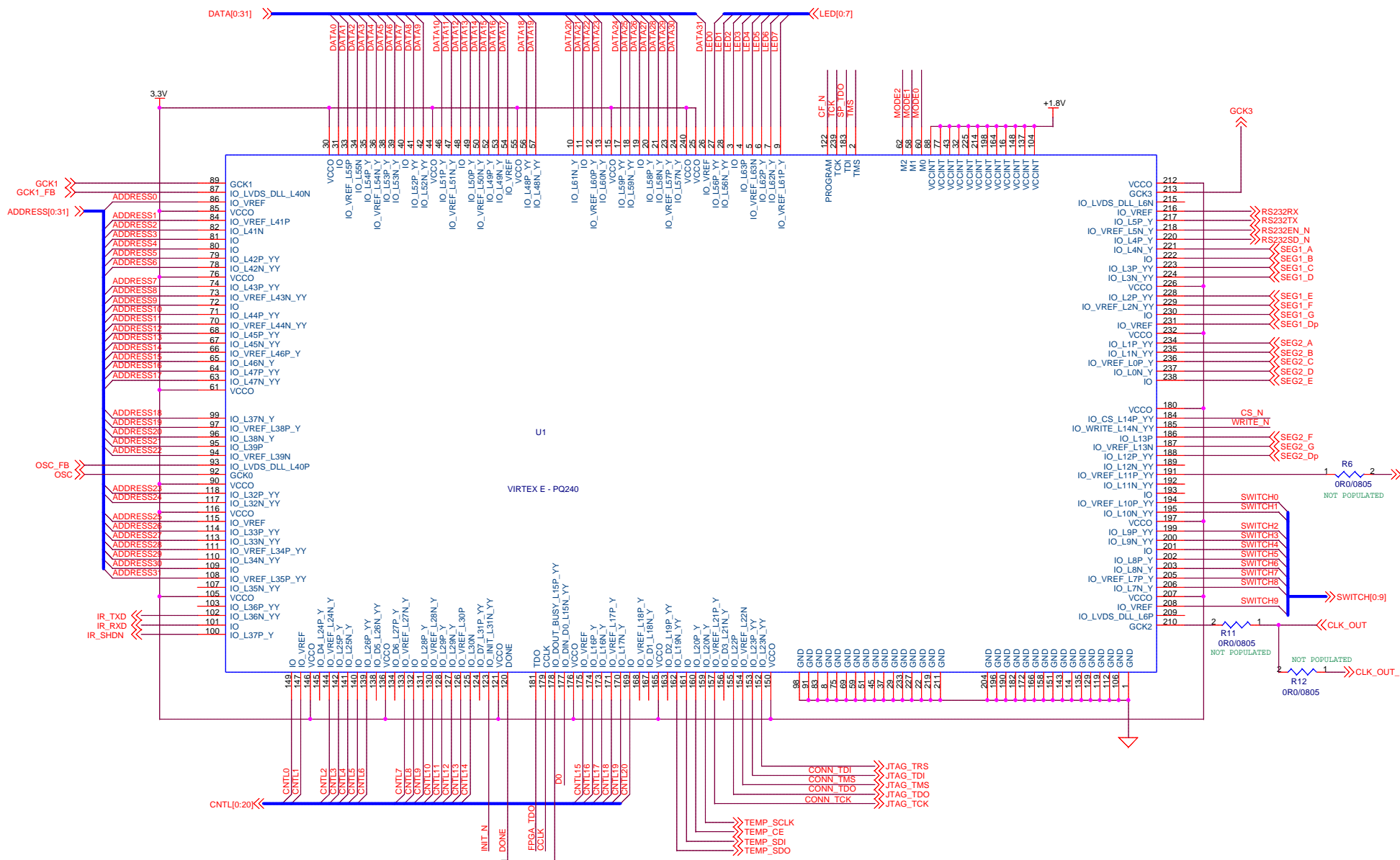
Avnet is not responsible for typographical or other errors or omissions or for direct, indirect, incidental or consequential damages related to this material or resulting from its use. Avnet makes no warranty or representation respecting this material, which is provided on an "AS IS" basis. AVNET HEREBY DISCLAIMS ALL WARRANTIES OR LIABILITY OF ANY KIND WITH RESPECT THERETO, INCLUDING, WITHOUT LIMITATION, REPRESENTATIONS REGARDING ACCURACY AND COMPLETENESS, ALL IMPLIED WARRANTIES AND CONDITIONS OF MERCHANTABILITY, SUITABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TITLE AND/OR NON-INFRINGEMENT. This material is not designed, intended or authorized for use in medical, life support, life sustaining or nuclear applications or applications in which the failure of the product could result in personal injury, death or property damage. Any party using or selling products for use in any such applications do so at their sole risk and agree that Avnet is not liable, in whole or in part, for any claim or damage arising from such use, and agree to fully indemnify, defend and hold harmless Avnet from and against any and all claims, damages, loss, cost, expense or liability arising out of or in connection with the use or performance of products in such applications.

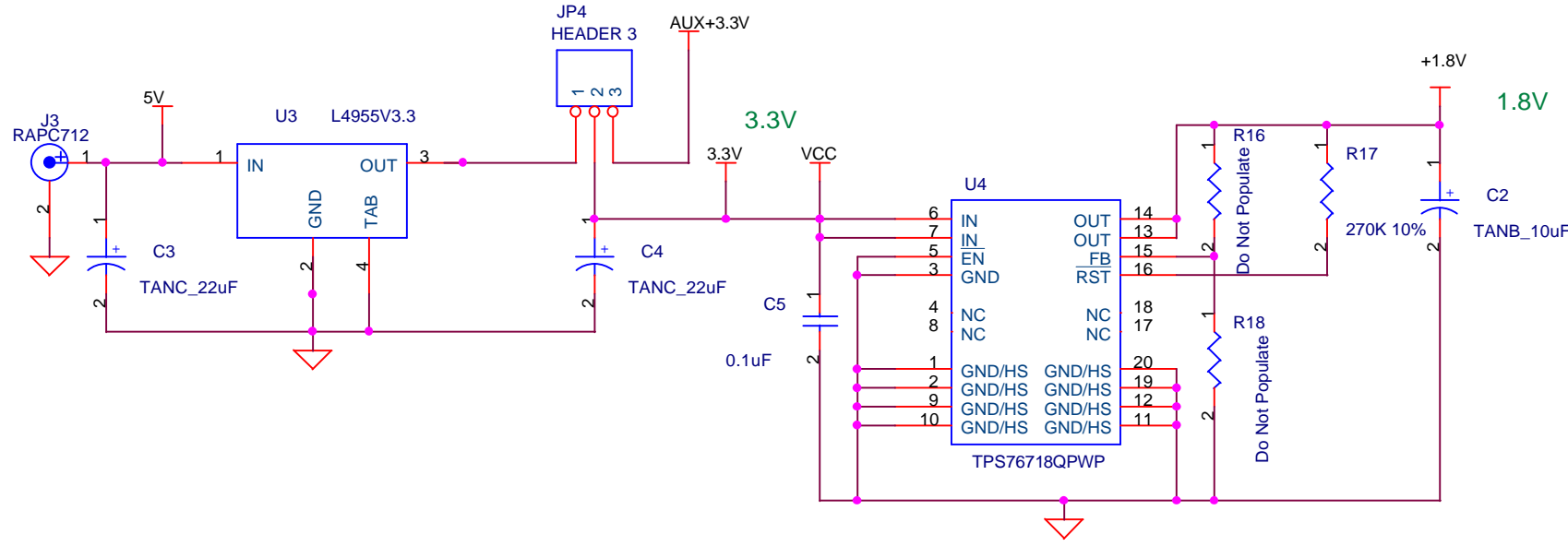


LIT# ADS-001207

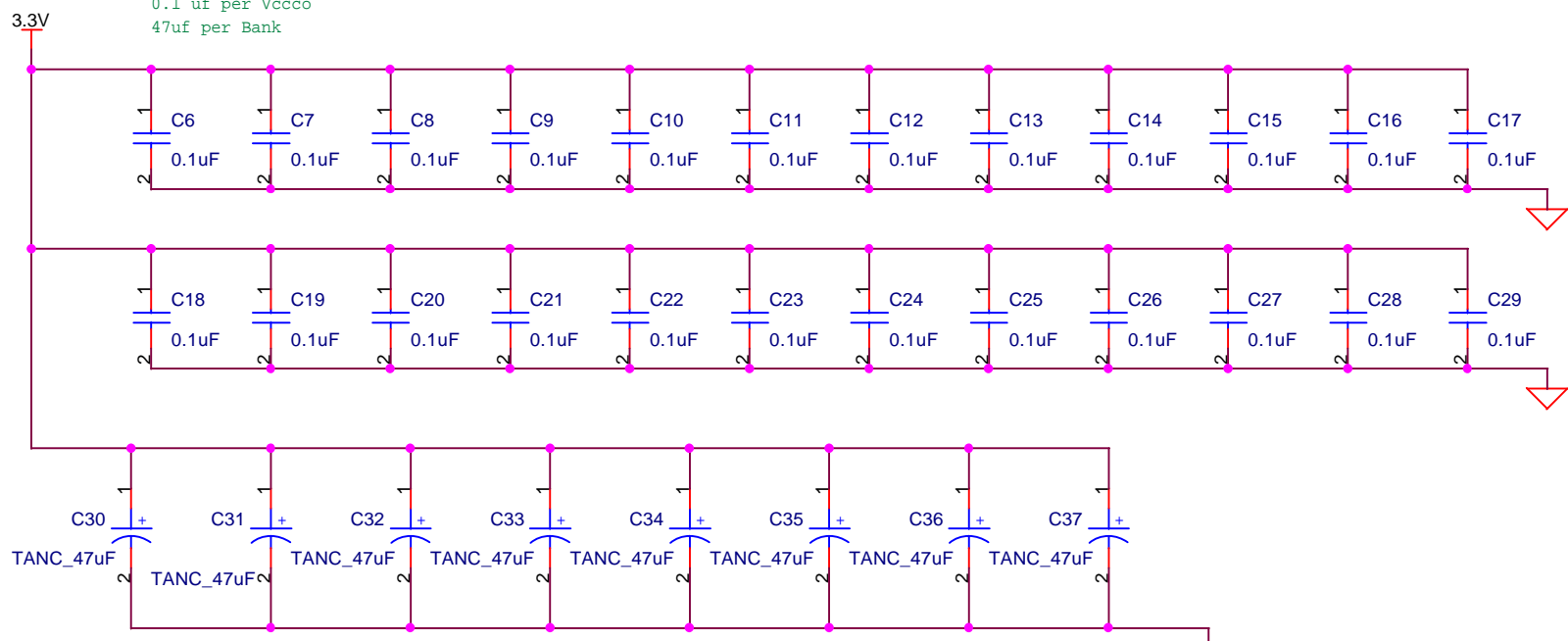
Avnet, Inc. Design Services		Copyright 2000
Title Mini-Virtex-E Board - Lead Sheet		
Size B	Document Number H394-XLX5-MVE-1002	Rev A
Date:	Tuesday, October 17, 2000	Sheet 1 of 6



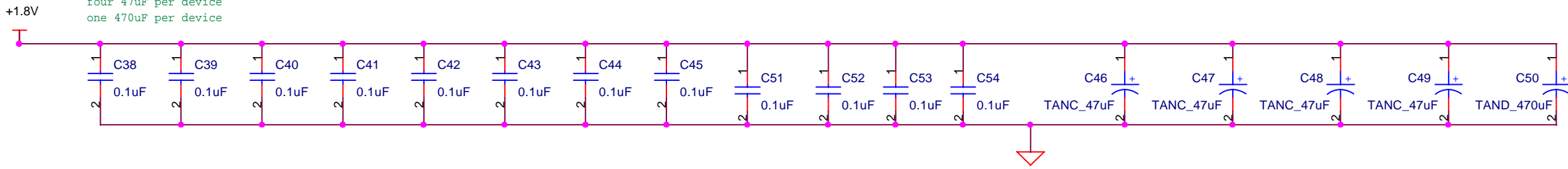




Virtex-E Decoupling Caps  
 0.1 uf per Vccco  
 47uf per Bank



Virtex-E Decoupling Caps  
 0.1uf per Vccint  
 four 47uF per device  
 one 470uF per device



**AVNET, INC. CONFIDENTIAL**

Avnet, Inc. Design Services		Copyright 2000
Title Mini-Virtex-E Board - Power		
Size B	Document Number H394-XLX5-MVE-1002	Rev A
Date:	Tuesday, October 17, 2000	Sheet 3 of 6

