

2

The MOS device

This chapter presents the CMOS transistor, its layout, static characteristics and dynamic characteristics. The vertical aspect of the device and the three dimensional sketch of the fabrication are also described.

The MOS device

The MOS transistor is basically a switch. When used in logic cell design, it can be *on* or *off*. When *on*, a current can flow between drain and source. When *off*, no current flow between drain and source. The MOS is turned on or off depending on the gate voltage. In CMOS technology, both n-channel (or nMOS) and p-channel MOS (or pMOS) devices exist. The nMOS and pMOS symbols are reported below. The n-channel MOS is built using polysilicon as the gate material and N+ diffusion to build the source and drain. The p-channel MOS is built using polysilicon as the gate material and P+ diffusion to build the source and drain. The symbols for the ground voltage source (0 or VSS) and the supply (1 or VDD) are also reported in figure 2-1.

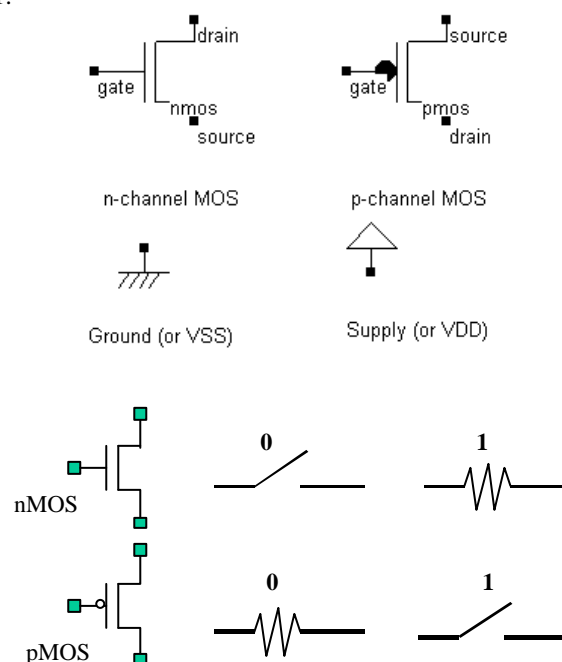


Fig. 2-1: the MOS symbol and switch

As illustrated in figure 2-2, the n-channel MOS device requires a logic value 1 (or a supply VDD) to be on. In contrary, the p-channel MOS device requires a logic value 0 to be on. When the MOS device is on, the link between the source and drain is equivalent to a resistance. The order of range of this 'on' resistance is 100Ω - $5K\Omega$. The 'off' resistance is considered infinite at first order, as its value is several $M\Omega$.

Logic Simulation of the MOS

At logic level, the MOS is considered as a simple switch. Moreover, the logic switch is unidirectional, meaning that the logic signal always flows from the source to the drain. This major restriction has no physical background. In reality, the current may flow both ways. The reason why the logic MOS device enables the signal to propagate only from source to drain is purely a software implementation problem. In the logic simulator of DSCH2, an arrow indicates whether or not the current flows, and its direction (Figure 2.2). When the device is OFF, the drain keeps its last logic value, thus acting as an elementary memory.

Notice that you cannot pass any logic information from the drain to the source. Such a circuit would fail.

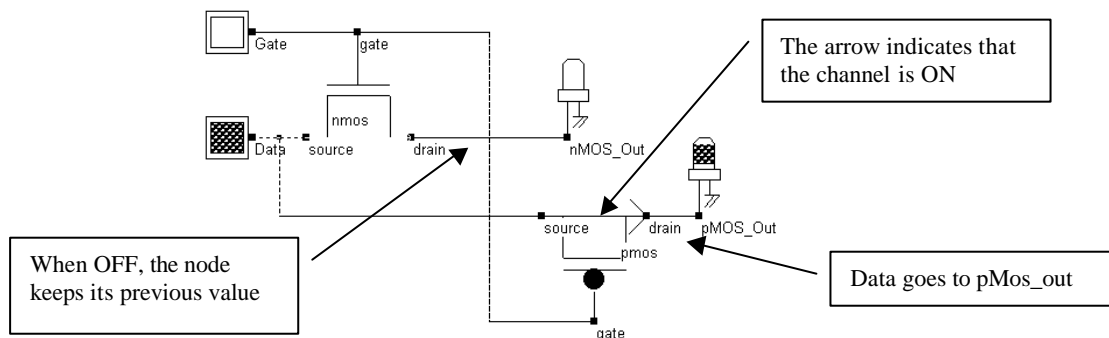


Fig. 2-2: the logic simulation of the MOS device (*MosExplain.SCH*)

MOS layout

We use MICROWIND2 to draw the MOS layout and simulate its behavior.

- ❶ Go to the directory in which the software has been copied (By default MICROWIND2)
- ❷ Double-click on the MicroWind2 icon

The MICROWIND2 display window includes four main windows: the main menu, the layout display window, the icon menu and the layer palette. The layout window features a grid, scaled in lambda (λ) units. The lambda unit is fixed to half of the minimum available lithography of the technology. The default technology is a CMOS 6-metal layers $0.25\mu\text{m}$ technology, consequently lambda is $0.125\mu\text{m}$.

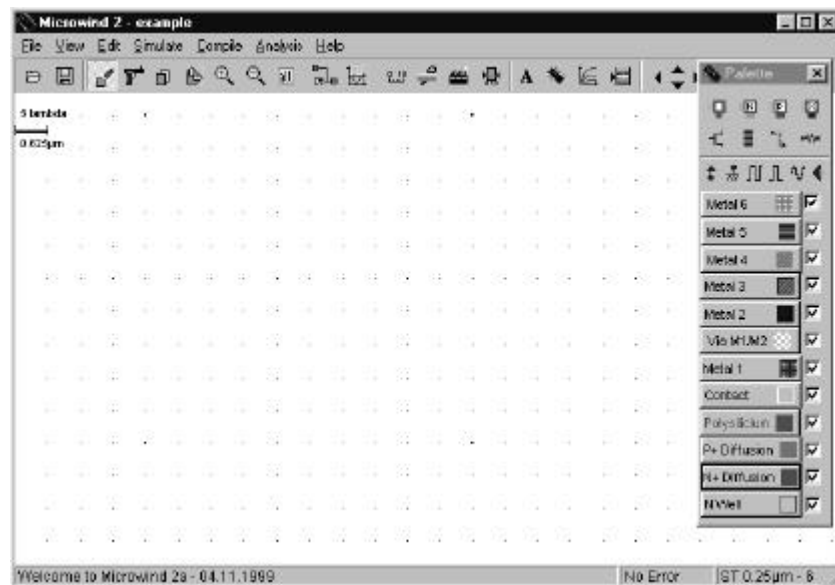


Fig. 2-3 The MICROWIND2 window as it appears at the initialization stage..

The palette is located in the lower right corner of the screen. A red color indicates the current layer. Initially the selected layer in the palette is polysilicon. By using the following procedure, you can create a manual design of the n-channel MOS.

- ❶ Fix the first corner of the box with the mouse. While keeping the mouse button pressed, move the mouse to the opposite corner of the box. Release the button. This creates a box in polysilicon layer as shown in Figure 2. The box width should not be inferior to 2λ , which is the minimum width of the polysilicon box.
- ❷ Change the current layer into N+ diffusion by a click on the palette of the Diffusion N+ button. Make sure that the red layer is now the N+ Diffusion. Draw a n-diffusion box at the bottom of the drawing as in Figure 2-4. N-diffusion boxes are represented in green. The intersection between diffusion and polysilicon creates the channel of the nMOS device.

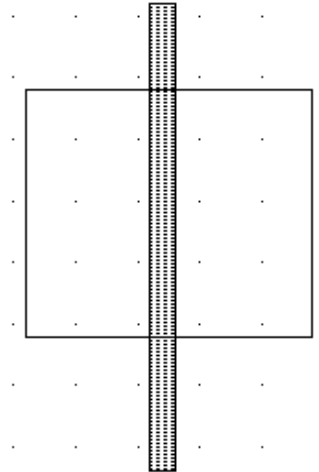


Fig. 2-4. Creating the N-channel MOS transistor

Vertical aspect of the MOS



Click on this icon to access *process simulation* (Command **Simulate** → **Process section in 2D**). The cross-section is given by a click of the mouse at the first point and the release of the mouse at the second point.

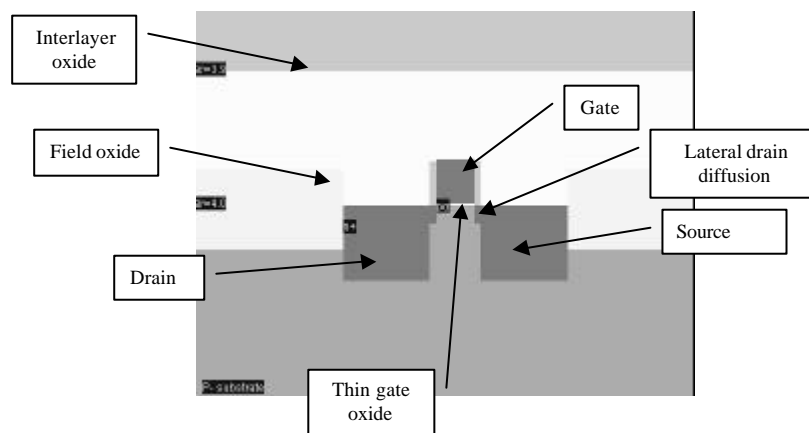


Fig. 2-5. The cross-section of the nMOS devices.

In the example of Figure 2-5, three nodes appear in the cross-section of the n-channel MOS device: the gate (red), the left diffusion called *source* (green) and the right diffusion called *drain* (green), over a substrate (gray). A thin oxide called the gate oxide isolates the gate. Various steps of oxidation have lead to stacked oxides on the top of the gate.

The physical properties of the source and of the drain are exactly the same. Theoretically, the source is the origin of channel impurities. In the case of this nMOS device, the channel impurities are the electrons. Therefore, the source is the diffusion area with the lowest voltage. The polysilicon gate floats over the channel, and splits the diffusion into 2 zones, the source and the drain. The gate controls the current flow from the drain to the source, both ways. A high voltage on the gate attracts electrons below the gate, creates an electron channel and enables current to flow. A low voltage disables the channel.

The lateral drain diffusion is a small region of lightly doped diffusion, at the interface between the drain/source and the channel. A light doping reduces the local electrical field between the drain/source and gate and prevents from oxide breakdown.

The permittivity of the field oxide is not always the same than the interlayer oxide. To reduce lateral coupling effects between conductors, a low permittivity dielectric, also called 'low K', has recently being introduced.

Static Mos Characteristics



Click on the *MOS characteristics* icon. The screen shown in Figure 2-6 appears. It represents the I_d/V_d static characteristics of the nMOS device.

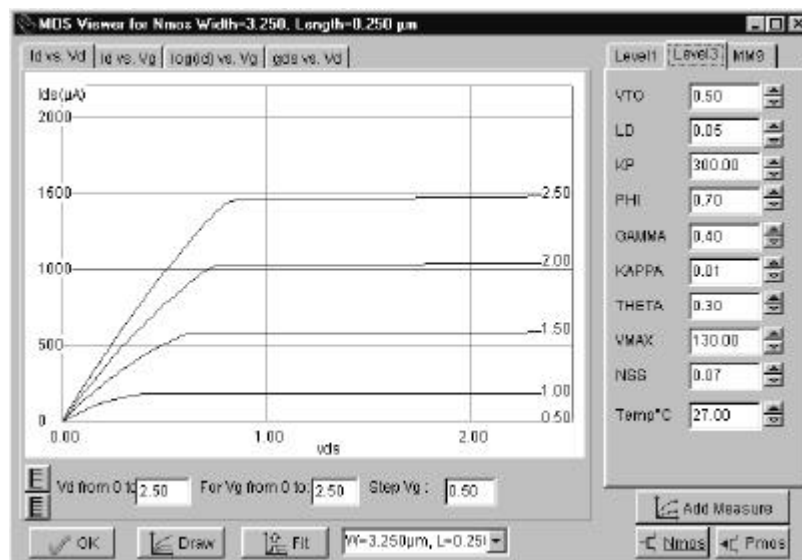
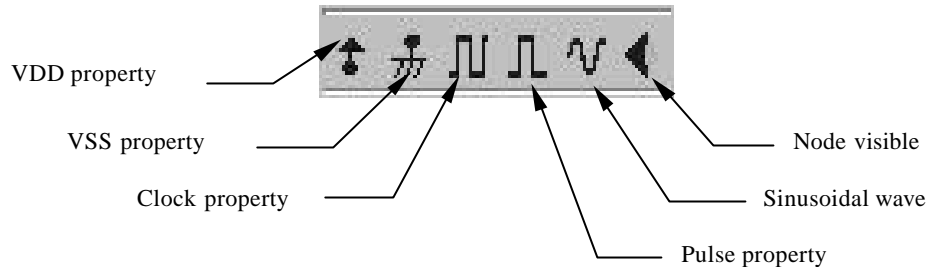


Fig. 2-6. N-Channel MOS characteristics.

The MOS size (width and length of the channel situated at the intersection of the polysilicon gate and the diffusion) has a strong influence on the value of the current. In Figure 2-6, the MOS width is $3.25\mu\text{m}$ and the length is $0.25\mu\text{m}$. A high gate voltage ($V_g = 2.5\text{V}$) corresponds to the highest I_d/V_d curve. For $V_g = 0$, no current flows. A maximum current around 1.5mA is obtained for $V_g = 2.5\text{V}$, $V_d = 2.5\text{V}$, with $V_s = 0.0$. The MOS parameters correspond to SPICE Level 3. A tutorial on MOS model parameters is proposed later in this chapter.

Dynamic MOS behavior

This paragraph concerns the dynamic simulation of the MOS to exhibit its switching properties. The most convenient way to operate the MOS is to apply a clock to the gate, another to the source and to observe the drain. The summary of available properties that can be added to the layout is reported below.



- 1 Apply a clock to the gate. Click on the Clock icon and then, click on the polysilicon gate. The clock menu appears again. Change the name into « Vgate » and click on OK to apply a clock with 2.1ns period (1ns at 0, 50ps rise, 1ns at 1, 50ps fall).

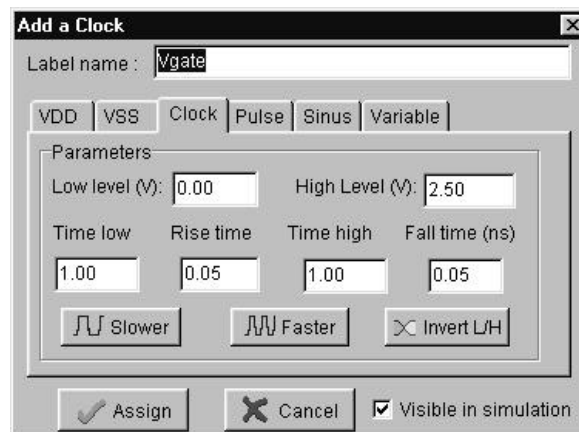


Fig. 2-7. The clock menu.

- 1 Apply a clock to the drain. Click on the Clock icon, click on the left diffusion. The Clock menu appears. Change the name into « Vdrain » and click on OK. A default clock with 4.2ns period is generated. The Clock property is sent to the node and appears at the right hand side of the desired location with the name « Vdrain ».
- 2 Watch the output: Click on the Visible icon and then, click on the right diffusion. Click OK. The Visible property is then sent to the node. The associated text « s1 » is in italic, meaning that the waveform of this node will appear at the next simulation.



- 3 Always save **BEFORE** any simulation. The analog simulation algorithm may cause run-time errors leading to a loss of layout information. Click on **File -> Save as**. A new window

appears, into which you enter the design name. Type, for example, **myMos**. Then click on 'Save'. The design is saved under that filename.

Analog Simulation

Click on **Simulate** → **Start Simulation**. The timing diagrams of the nMOS device appear, as shown in Figure 2-8.

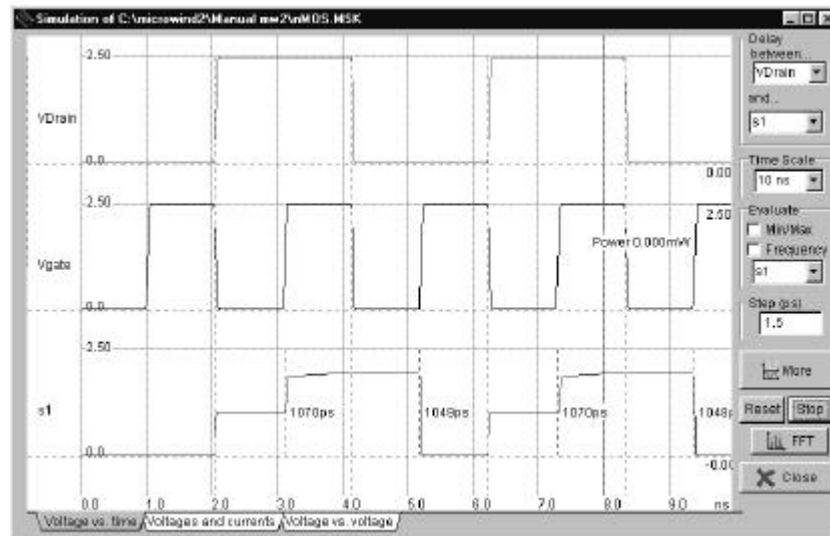


Fig.2- 8. Analog simulation of the MOS device.

When the gate is at zero, no channel exists so the node s1 is disconnected from the drain. When the gate is on, the source copies the drain. It can be observed that the nMOS device drives well at zero but poorly at the high voltage. The highest value of s1 is around 2.0V, that is VDD minus the threshold voltage. This means that the n-channel MOS device do not drives well logic signal 1, as summarized in figure 2-9. Click on **More** in order to perform more simulations. Click on **Close** to return to the editor.

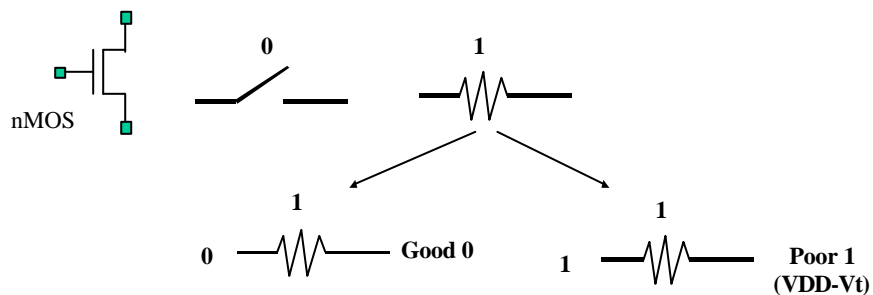
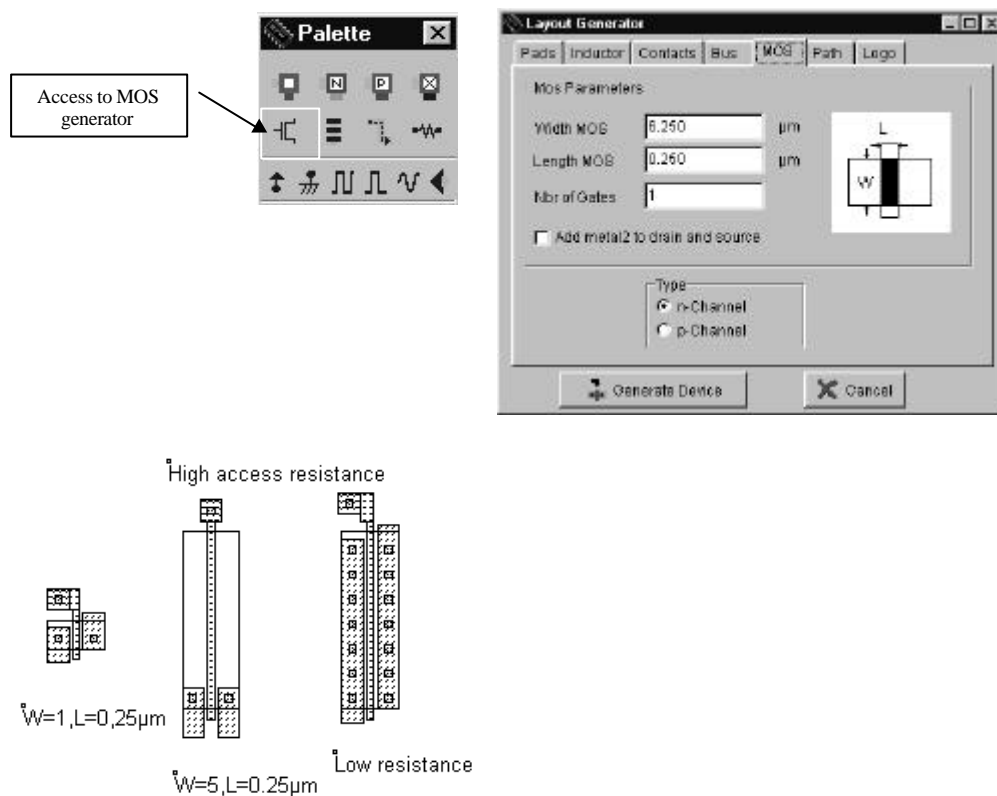


Fig.2- 9. The nMOS device behavior summary

Layout considerations

The safest way to create a MOS device is to use the MOS generator. In the palette, click the MOS generator icon. A window appears as reported below. The programmable parameters are the MOS width, length, the number of gates in parallel and the type of device (n-channel or p-channel). By default metal interconnects and contacts are added to the drain and source of the MOS. You may add a supplementary metal2 interconnect on the top of metal 1 for drain and source.



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Fig.2-10. Analog simulation of the MOS device.

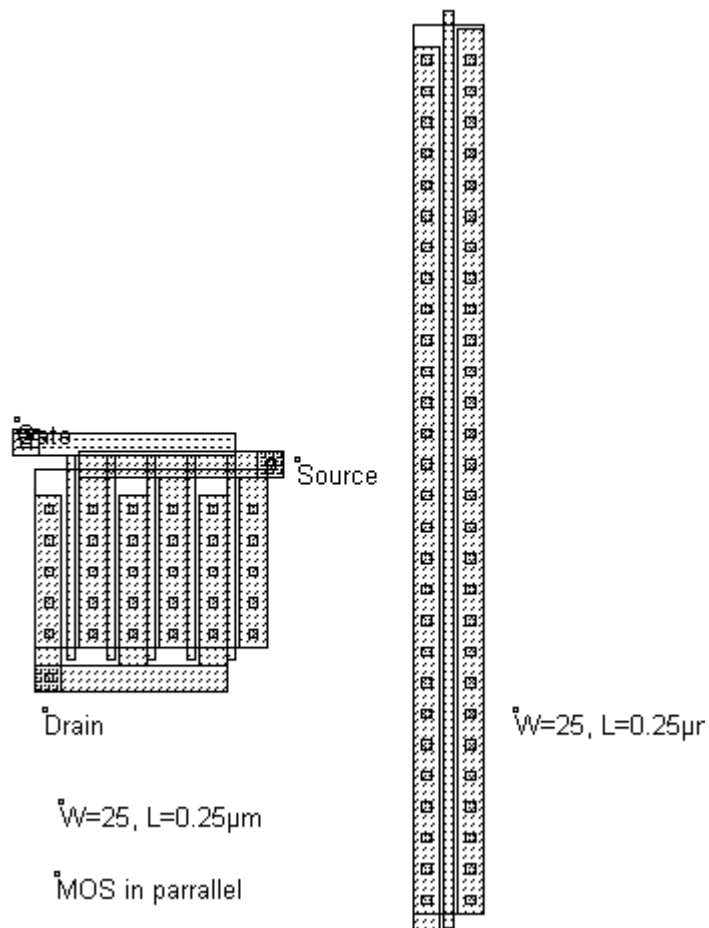


Fig.2-11. Various layout aspects of the MOS device.

The MOS Model 1

For the evaluation of the current I_{ds} between the drain and the source as a function of V_d, V_g and V_s , you may use the old but nevertheless simple MODEL 1 described below.

MODE	CONDITION	EXPRESSION FOR THE CURRENT I_{ds}
CUT-OFF	$V_{gs} < 0$	$I_{ds} = 0$
LINEAR	$V_{ds} < V_{gs} - V_t$	$I_{ds} = KP \frac{W}{L} ((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2})$
SATURATED	$V_{ds} > V_{gs} - V_t$	$I_{ds} = KP/2 \frac{W}{L} (V_{gs} - V_t)^2$


With:

$$v_t = VTO + GAMMA + \sqrt{(PHI - vb)} - \sqrt{PHI}$$

MOS MODEL 1 PARAMETERS		
PARAMETER	DEFINITION	TYPICAL VALUE 0.25μm
		NMOS pMOS

VTO	Threshold voltage	0.4V	-0.4V
KP	Transconductance coefficient	$300\mu\text{A}/\text{V}^2$	$120\mu\text{A}/\text{V}^2$
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	$0.4\text{ V}^{0.5}$	$0.4\text{ V}^{0.5}$
W	MOS channel width	0.5-20 μm	0.5-40 μm
L	MOS channel length	0.25 μm	0.25 μm

Let us compare the simulation and the measurement, for a 10x10 μm device.

- ❶ Click **Simulate** → **Mos characteristics** (Or the icon )
- ❷ Click **Add Measure**.
- ❸ Select the data file **“Nb10x0,25.MES”**. The “N” means an n-channel MOS device. The “b” corresponds to a chip called “BETA” fabricated in 0.25 μm technology by ST-Microelectronics. The values 10x0,25 means W=10 μm , L=0.25 μm .
- ❹ Select “Level 1” in the parameter list to compare LEVEL1 simulated characteristics with the measurements.

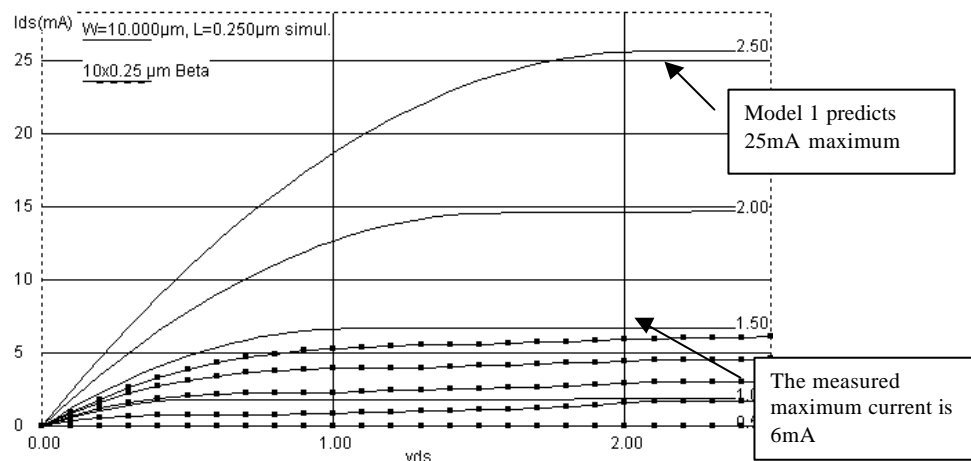


Fig.2- 12: The model 1 predict a current 4 times higher than the measurement

When dealing with sub-micron technology, the model 1 is more than 4 times too optimistic regarding current prediction, compared to real-case measurements, as shown above for a 10x0,25 μm n-channel MOS.

The MOS Model 3

For the evaluation of the current I_{ds} as a function of V_d, V_g and V_s between Drain and Source, we commonly use the following equations, close from the SPICE model 3 formulations. The formulations are derived from the model 1 and take into account a set of physical limitations in a semi-empirical way.

CUT-OFF MODE. $V_{gs} < 0$

$$I_{ds} = 0$$

NORMAL MODE. $V_{gs} > V_{on}$

$$I_{ds} = K_{eff} \frac{W}{L_{EFF}} (1 + KAPPA \cdot v_{ds}) V_{de} \left((V_{gs} - v_{th}) - \frac{V_{de}}{2} \right)$$

with

$$v_{on} = 1.2 \cdot v_{th}$$

$$v_{th} = V_{TO} + GAMMA(\sqrt{PHI} - \sqrt{v_b} - \sqrt{PHI})$$

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$v_{dsat} = v_c + v_{sat} - \sqrt{v_c^2 + v_{sat}^2}$$

$$v_{sat} = v_{gs} - v_{th}$$

$$v_c = V_{MAX} \frac{L_{EFF}}{0.06}$$

$$L_{EFF} = L - 2 \cdot LD$$

$$K_{eff} = \frac{KP}{(1 + THETA (v_{gs} - v_{th}))}$$

SUB-THRESHOLD MODE. $V_{gs} < V_{on}$. V_{ds} is replaced by v_{on} in the above equations.

$$I_{ds} = I_{ds}(v_{on}, v_{ds}) e^{\frac{q(v_{gs} - v_{on})}{nkT}}$$

TEMPERATURE EFFECTS

$$\mu_n = \mu_{n0} (T-300) e^{-1.5}$$

$$\mu_p = \mu_{p0} (T-300) e^{-1.5}$$

$$v_t = v_{t0} - 0.002(T-300)$$

MOS MODEL 3 PARAMETERS			
PARAMETER	DEFINITION	TYPICAL VALUE 0.25μm	
		NMOS	pMOS
VTO	Threshold voltage	0.4V	-0.4V
KP	Transconductance coefficient	300μA/V ²	120μA/V ²
PHI	Surface potential at strong inversion	0.3V	0.3V
LD	Lateral diffusion into channel	0.01μm	0.01μm
GAMMA	Bulk threshold parameter	0.4 V ^{0.5}	0.4 V ^{0.5}
KAPPA	Saturation field factor	0.01 V ⁻¹	0.01 V ⁻¹
VMAX	Maximum drift velocity	150Km/s	100Km/s
THETA	Mobility degradation factor	0.3 V ⁻¹	0.3 V ⁻¹
NSS	Subthreshold factor	0.07 V ⁻¹	0.07 V ⁻¹
W	MOS channel width	0.5-20μm	0.5-40μm
L	MOS channel length	0.25μm	0.25μm

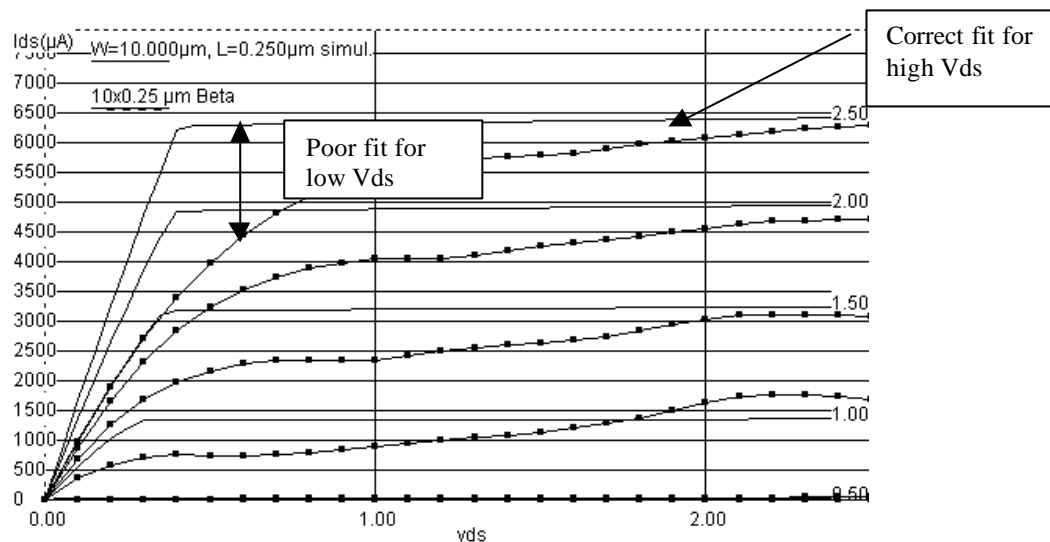


Fig.2- 13: The model 3 predicts well the maximum current but overestimates the current at small V_{ds}

Select “Level 3” in the parameter list to compare LEVEL 3 simulated characteristics with the measurements. The screen of figure 2-13 displays the I_d/V_d simulation of the $10 \times 0.25 \mu\text{m}$ nMOS device. A good fit is observed for high V_{ds} , but for low V_{ds} the error is about 30%.

FITTING THE MOS MODEL 3

- ❶ Load measurements concerning $10 \times 10 \mu\text{m}$ or $20 \times 20 \mu\text{m}$ devices first. You should always start with measurements for a device with a very large width and length. The second order effects are reduced in such devices. In $0.25 \mu\text{m}$, a $10 \times 10 \mu\text{m}$ device is a good candidate to start fitting the model.
- ❷ Select the curve I_d/V_g by a click on **I_d vs. V_g** . The curve shown in Figure 2-14 is used to fit VTO, KP and GAMMA. Act on VTO cursors in order to shift the curves right or left, KP to adjust the slope, and GAMMA to fit the spacing between curves.

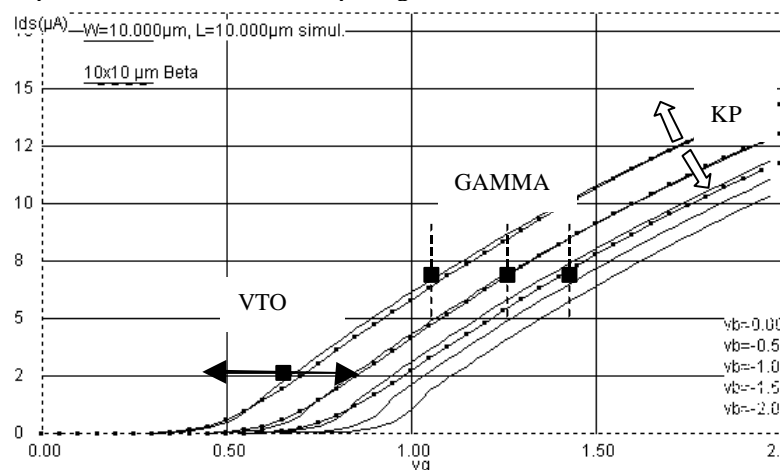


Fig. 2-14. The I_d/V_g curves used to fit KP, VTO and GAMMA (Nb10x10.MES)

- ③ Click on **Id vs. Vd**. Increase THETA to bend the curve in order to find a compromise.

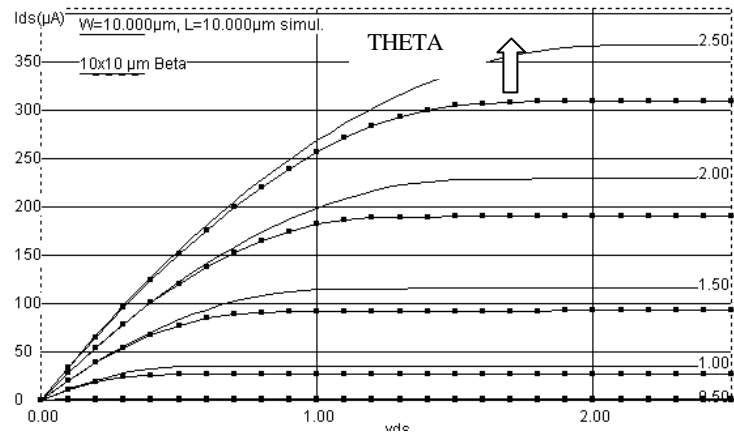


Fig. 2-15 . The I_d/V_d curves used to fit THETA (Nb10x10.MES)

- ④ Now load a short channel MOS device measurement (smallest length), for example $W=10\mu\text{m}$, $L=0.25\mu\text{m}$ (Nb10x0,25.MES). Click on **Id vs. Vg**. In figure 2-16, it can be seen that VTO or this device is higher than for the 10x10 μm device. Increase LD in order to fit the slope in the I_d/V_g curve, and adjust THETA to bend the current curves at high V_g .

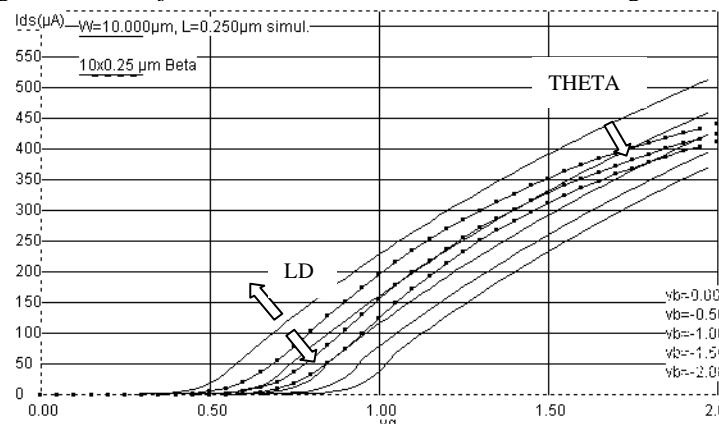


Fig. 2-16. The I_d/V_g curves on a small channel MOS used to fit LD and adjust THETA (Nb10x0,25.MES)

- ⑤ Click on **Id vs. Vd** (Figure 2-17). Adjust VMAX to fit the transition point between the linear and the saturated region according to the measurement. Next, adjust KAPPA to adapt the positive slope in the saturated region.

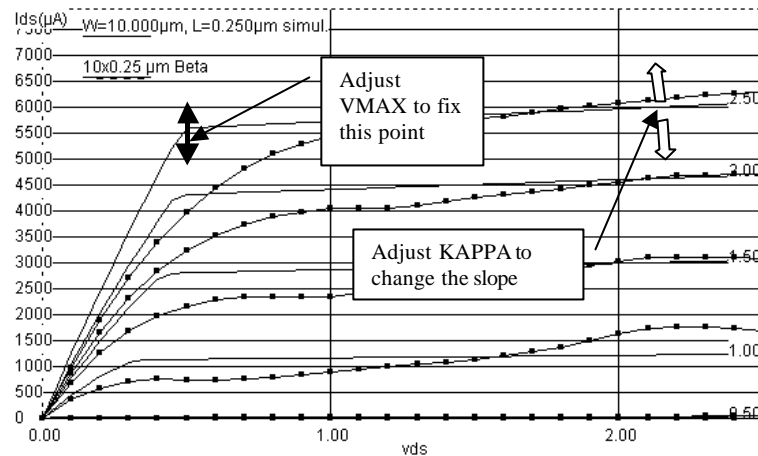


Fig. 2-17 . The I_d/V_d curves on a small channel MOS used to fit V_{MAX} and $KAPPA$ (Nb10x0,25.MES)

- ③ Click on **Id(log)/Vg** (Figure 2-18). Adjust the slope in sub-threshold mode using NSS.

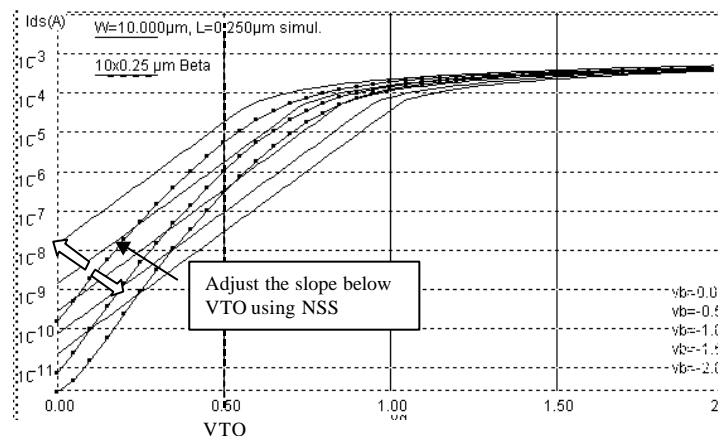


Fig. 2-18. Fitting the MOS model in the sub-threshold region (Nb10x0,25.MES)

The step-by-step procedure to build an accurate MOS model based on a set of measurements has been described. The experimental data concerning a MOS device with large width and large length is used first, to fix basic parameters. Then the MOS model is tuned for small channel device measurements. Unfortunately, the resulting model may not fit well in all operating regions, for all device sizes. This is why the industrial approach for building model parameters is based on optimization algorithms.

The MOS Model 9

The MM9 model is a compact MOS-transistor model, intended for the simulation of circuit behavior with emphasis on analog applications. This model gives a complete description of all transistor-action-related quantities. The equations describing these quantities are based on the gradual-channel approximation with a number of first-order corrections for small-size effects. The consistency is maintained by using the same

carrier-density and electrical-field expressions in the calculation of all model quantities. The continuity of the derivatives of currents and charges has been a point of special emphasis. The basic current equation in linear mode is reported in (2).

$$I_{DS} = b \cdot G_3 \cdot \frac{V_{GT3} \cdot V_{DS1} - \left(\frac{1+d_1}{2} \right) \cdot V_{DS1}^2}{\left\{ 1 + q_1 \cdot V_{GT1} + q_2 \cdot (U_s - U_{s0}) \right\} \cdot (1 + q_3 \cdot V_{DS1})}$$

Especially the description of the transition from weak to strong inversion and also of the transition from linear to saturation have been thoroughly investigated. The model philosophy is to combine the default parameter value with a channel length dependence and a channel width dependence, as illustrated below.

$$q_i = \tilde{q}_i + \left(\frac{1}{L_E} - \frac{1}{L_{ER}} \right) \cdot S_{L;q_i} + \left(\frac{1}{W_E} - \frac{1}{W_{ER}} \right) \cdot S_{W;q_i}$$

The MOS model 9 basic parameters are extracted from the static measurement of current versus voltage NMOS and PMOS transistors of different sizes. From I-V and C-V characterizations of individual test devices, using a Semiconductor Parameter Analyzer (such as, for example, HP 4155A, 4156A or 4140B), the device model parameters are extracted. Consequently, circuit simulations based on the model and the extracted parameters can be performed for comparison purpose. In Figure xxx, the list of devices implemented in a 0.35 μ m technology is reported. The devices are drawn in a width/length diagram showing that at least three MOS devices have the same width, and three others have the same length. This is mandatory to fit accurately the width and length depend parameters.

CODE	W x L	COMMENTS
A	80x0.25	typical buffer
B	10x10	MOS ref.
C	10x2.0	Low power logic
D	1.0x0.25	W dependency
E	10x0.25	L dependency
F	1.0x2.0	to cover the space

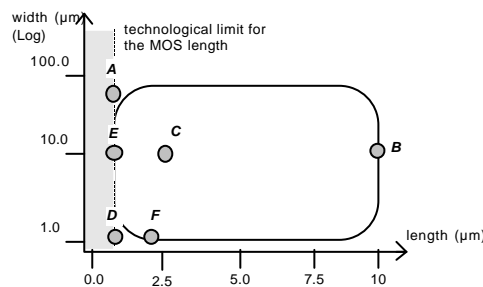


Fig 2-20: MOS sizes chart in 0.25 μ m CMOS Technology

FITTING THE MOS MODEL 9

In the following paragraph the MOS model 9 extraction technique is detailed. The model relies on a reference MOS device with a large length : we use a $10 \times 10 \mu\text{m}$ device in our case. The extraction sequence is split into four steps as shown in figure 2-21.

- ① Determination of V_{TOR} , $BETSQ$ and $THET1R$ using the I_d/V_g characteristics of the $10 \times 10 \mu\text{m}$ reference device. V_{TOR} is the threshold voltage of the reference device, $BETASQ$ the gain factor illustrated by the slope of I_d with very small V_d (0.1V), and $THET1R$ is the mobility reduction factor which induces a current reduction compared to the ideal linear slope.
- ② Determination of KOR , $VS BX$ and $THET2R$. KOR and $VS BX$ act on the spacing between the characteristics for varying bulk voltage. The parameter $THET2R$ modifies the shape of the curve at high gate voltage and low bulk biasing.
- ③ Determination of MOR and $ZET1R$. The slope factor MOR for sub-threshold region is fitted in the I_D characteristics with Y axis in logarithmic scale. $ZET1R$ acts on the correction due to bulk biasing.
- ④ Using now the I_d/V_d curve, we determine the value of $THE3R$ corresponding to the mobility degradation in strong V_d s and high gate voltage.

Once the extraction of the parameters is completed for the reference MOS device, the four steps are repeated on a new device with the same width but a different length. Consequently, the length-dependent parameters are extracted. For example, the characteristics of the $10 \times 0.4 \mu\text{m}$ device (Code E) are used to fit the value of SLV_{TOR} , $SLTHET1R$, $SLTHET2R$, $SLKOR$ and $SLTHET3R$.

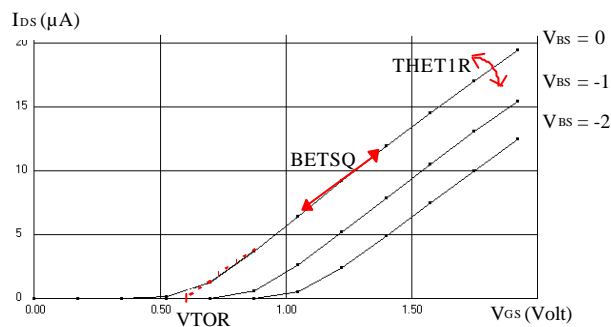


Fig. 2-21 : Step-by-step extraction for the reference device

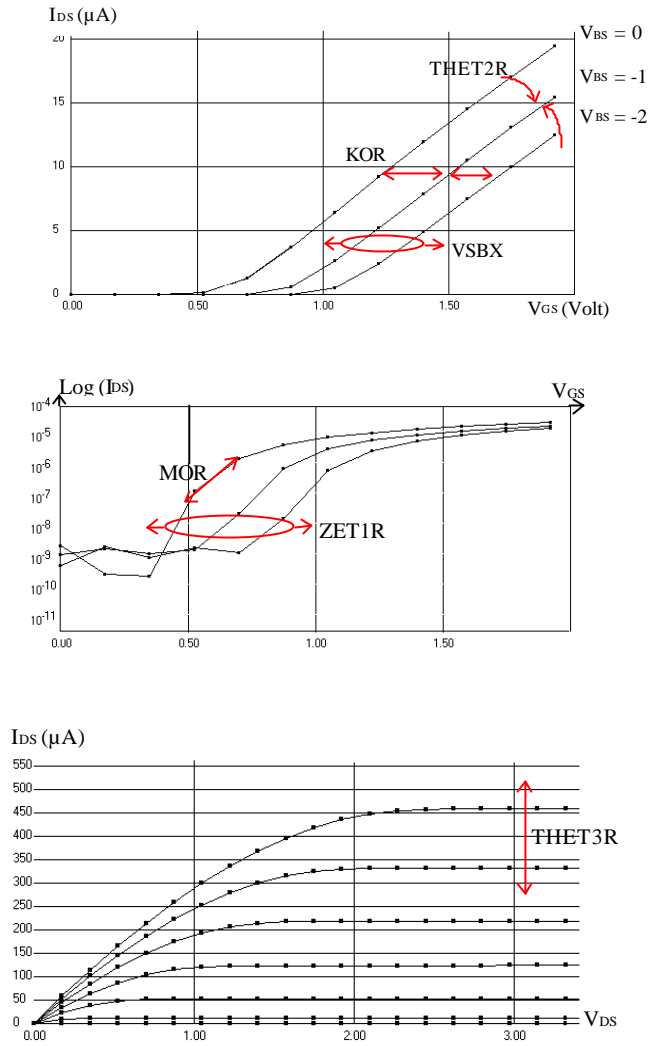


Fig. 2-22 : Step-by-step extraction for the reference device

Then the parameters which depend on the channel width W ($SWVTOR$, $SWTHET1R$, $SWTHET2R$, $SWKOR$ and $SWTHET3R$) are determined using for example the MOS device with a $1 \times 0.4 \mu m$ size (Code D). Details on the final aspect of the I_d/V_d characteristics for both sizes are reported in Figure 2-23. The MOS Model 9 gives a very accurate prediction of the current in all domains, for all available sizes of devices. The sequence is straightforward and do not require supplementary optimization steps to achieve a satisfactory result.

<to be added>

Fig. 2-23 : Fitting L -dependent parameters (top) on a $xxx0.25$ and W -dependent one (bottom) on a $1x0.25$.

The BSIM4 MOS Model

A MOS model developed by the University of Berkeley, called BSIM4, has been introduced in 2000. This model will soon be supported by Microwind2.

<Infos to be added>

Temperature effects on the MOS

The MOS device is sensitive to temperature. Two main parameters are concerned: the threshold voltage V_{TO} and the transconductance coefficient K_P that decrease with temperature increase. The physical background is the degradation of mobility of electrons and holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers. The modeling of the temperature effect is as follows:

$$K_P(T) = K_P(T_0) (T - T_0) e^{-1.5}$$

$$V_{TO}(T) = V_{TO}(T_0) - 0.002 (T - T_0)$$

With $T_0 = 300^\circ\text{K}$ generally

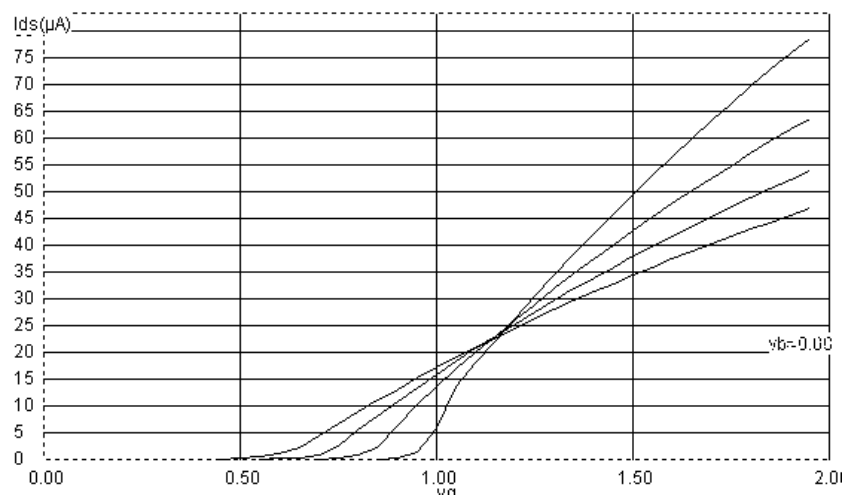


Fig. 2-24. Fitting the MOS model in the sub-threshold region (Nb10x0,25.MES)

To obtain the curve of figure 2-xxx, proceed as follows:



- ❶ Click the icon MOS characteristics
- ❷ Select one MOS in the design or click anywhere
- ❸ Select the curve I_d/V_g



- ❹ Enable the screen memory mode by a click on this icon.



- ❺ Change the temperature. The change in the slope is shown. You may reduce the number of I_d curves by putting a 0.0 in the field 'For V_b from 0 to :'.

In the case of logic circuits, the main consequence of temperature increase is the decrease of mobility, leading to slower transient performances. Thus, the propagation delay due to the gate is increased, as

illustrated in figure 2-25 on a 3-inverter ring oscillator. In the case of analog circuits, the threshold variation may also induce parasitic effects. There is a remarkable point at $V_{gs}=1.2V$ for which the current I_d is almost constant. Biasing the MOS device with $V_{gs}=1.2V$ would lead to a temperature-independent behavior. This property is used in some high performance applications.

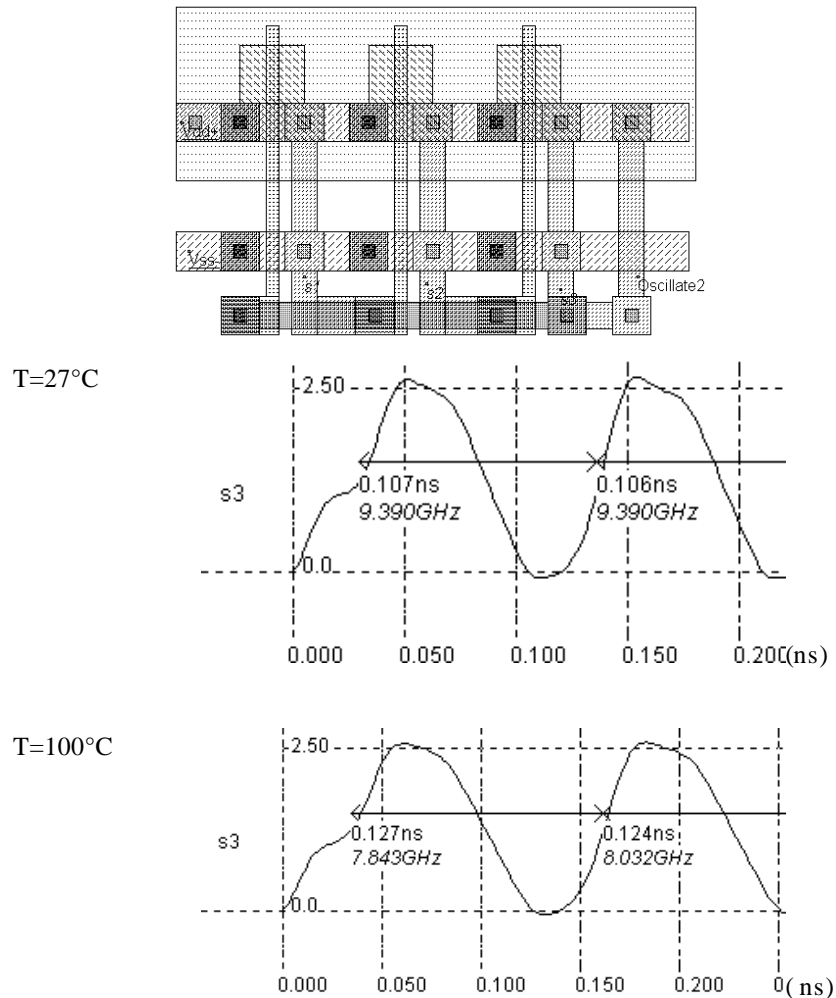


Fig. 2-25. Propagation delay increase with temperature.

In Microwind2, you can get access to temperature using the command **Simulate -> Simulation Parameters**. The screen below appears. The temperature is given in $^{\circ}C$.

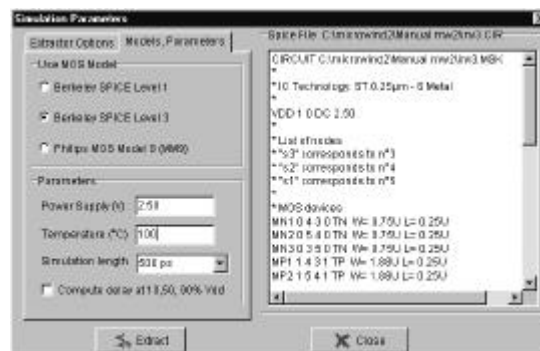


Fig. 2-26. Access to temperature within Microwind2.

High frequency behavior of the MOS

<text> Baker p 174

The transit frequency f_t is a parameter well representative of the technology. It corresponds to the frequency starting which the current i_d is lower than i_g . Thus, f_t is the frequency for which the current gain of the MOS device is unity. Based on the equations of level 1, an analytical approximation of f_t is reported below [Baker p 174].

$$f_t = \frac{K_p \cdot W}{2\mu \cdot L C_{gs}} (V_{gs} - V_t) \text{ with } C_{gs} \approx \frac{2}{3} (W L C_{ox})$$

with

K_p = technological parameter ($A \cdot V^{-2}$)

W = channel width (μm)

L = channel length (μm)

C_{gs} = gate to source capacitance (F)

V_{gs} = gate to source voltage (V)

V_t = threshold voltage

Replacing the value of C_{gs} in the expression of f_t , the transit frequency becomes independent of the channel width. For an n-channel MOS device, with $K_p=200\mu A/V^2$, $L=0.25\mu m$, $V_{gs}-V_t=0.1V$, $C_{ox}=4600aF/\mu m^2$, the value of f_t is around 30GHz.

A similar parameter, the cut-off frequency, is the frequency starting which a small voltage signal on the gate of the MOS device is no more amplified at the output. Let us consider the basic circuit of figure xxx below. The

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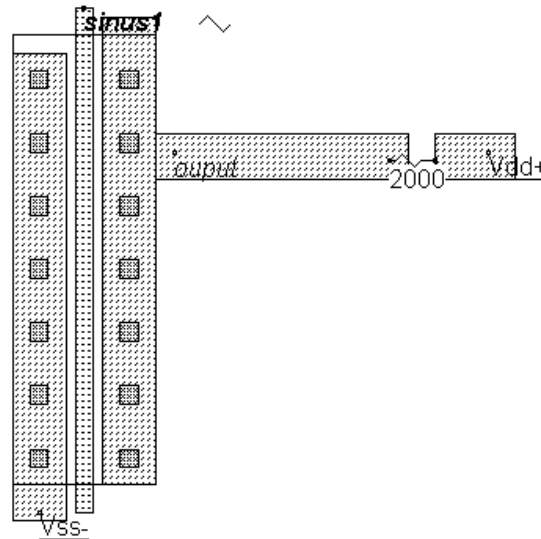


Fig. 2-27. Illustrating the cut-off frequency of the MOS device

The PMOS Transistor

The p-channel transistor simulation features the same functions as the n-channel device, but with opposite voltage control of the gate. For the nMOS, the channel is created with a logic 1 on the gate. For the pMOS, the channel is created for a logic 0 on the gate. Load the file "pmos.msk" and click the icon "MOS characteristics". The p-channel MOS simulation appears, as shown in Figure 2-28. Note that the pMOS gives approximately half of the maximum current given by the nMOS with the same device size. The highest current is obtained with the lowest possible gate voltage, that is 0.

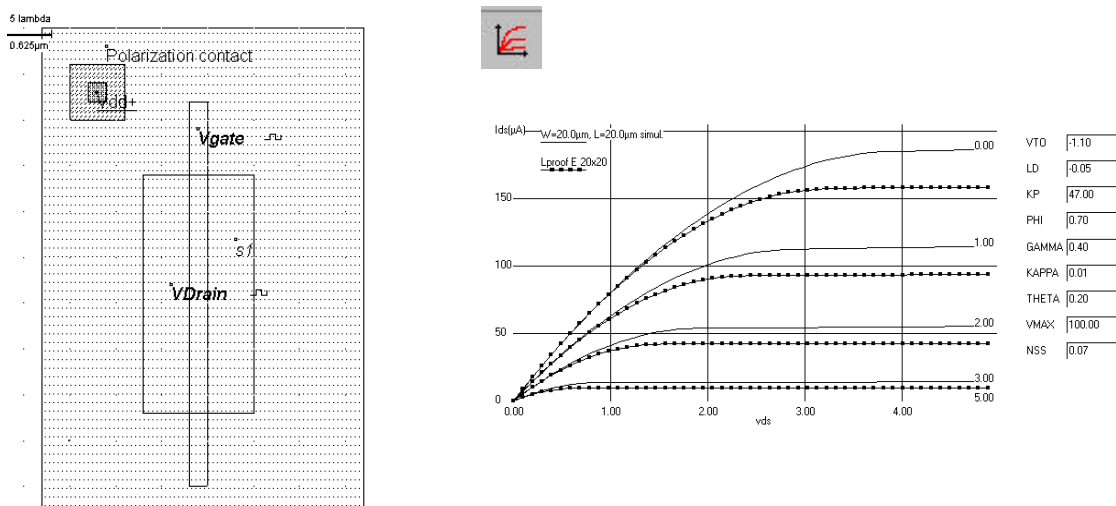


Fig. 2-28. Static simulation of the p-channel MOS (pMOS.MSK)

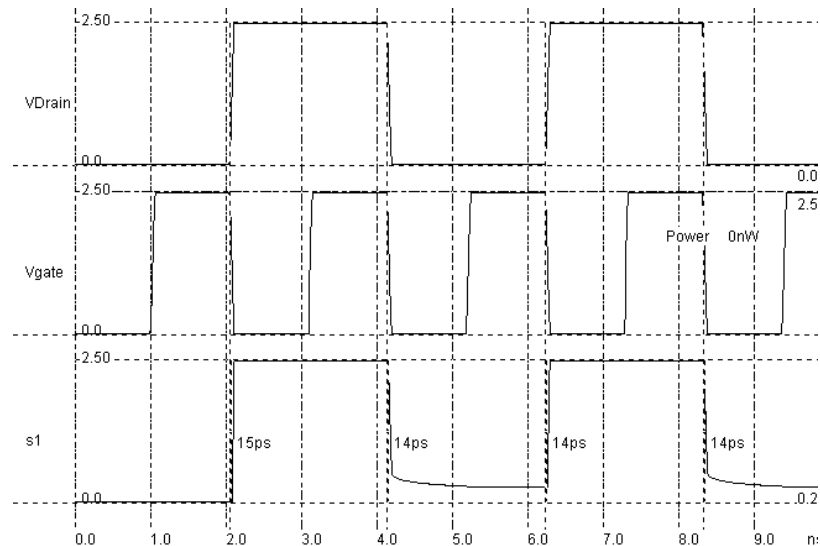


Fig. 2-29. Time domain simulation of the p-channel MOS (pMOS.MSK)

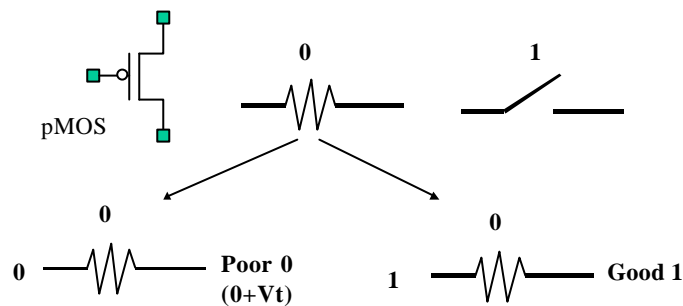


Fig. 2-30. Summary of the performances of a pMOS device

From the simulation of figure 2-29, we see that the pMOS device is able to pass well the logic level 1. But the logic level 0 is transformed into a positive voltage, equal to the threshold voltage of the MOS device. The summary of the p-channel MOS performances is reported in figure 2-30.

The Transmission Gate

Both NMOS devices and PMOS devices exhibit poor performances when transmitting one particular logic information. The nMOS degrades the logic level 1, the pMOS the logic level 0. Thus, a perfect pass gate can be constructed from the combination of nMOS and pMOS devices, leading to improved performances.

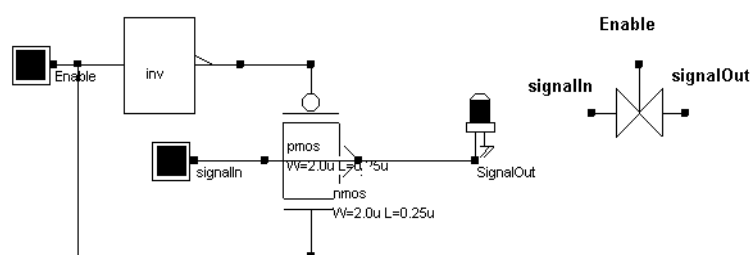


Fig. 2-31. The transmission gate

The transmission gate let a signal flow if Enable is asserted. To pass logic signals well, both a n-channel device and a p-channel device are used, as shown in figure 2-31. The main drawback is the need for two control signals Enable and /Enable, thus an inverter is usually required.

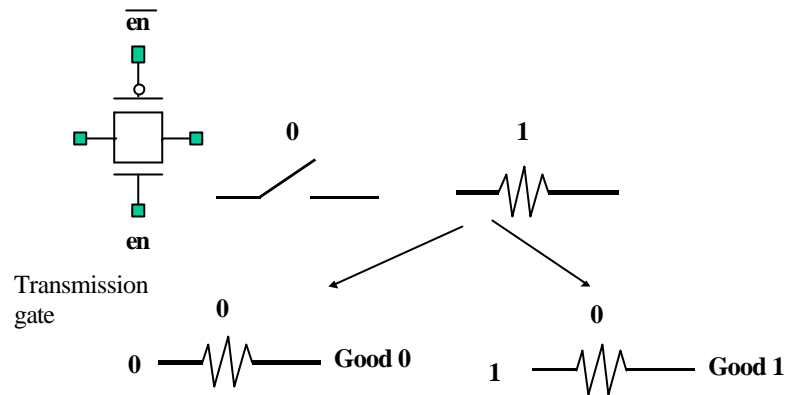


Fig. 2-32. The transmission gate used to pass logic signals

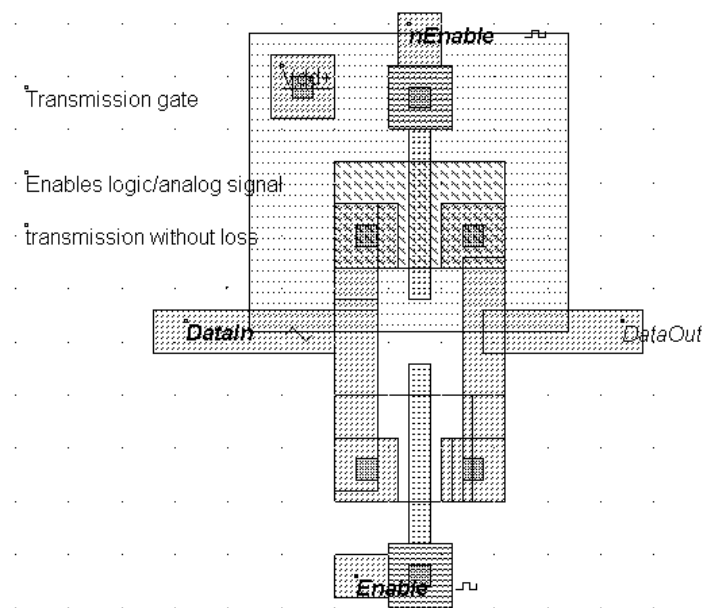


Fig. 2-33. Layout of the transmission gate (TGATE.MSK)

The layout of the transmission gate is reported in figure 2-33. The n-channel MOS is situated on the bottom the p-channel MOS on the top. Notice that the gate controls are not connected, as nEnable is the opposite of Enable. The operation of the transmission gate is illustrated in figure 2-34. A sinusoidal wave with a frequency of 2GHz is assigned to DataIn. With a zero on Enable (And a 1 on nEnable), the switch is off, and no signal is transferred. When Enable is asserted, the sinusoidal wave appears nearly identical to the output.

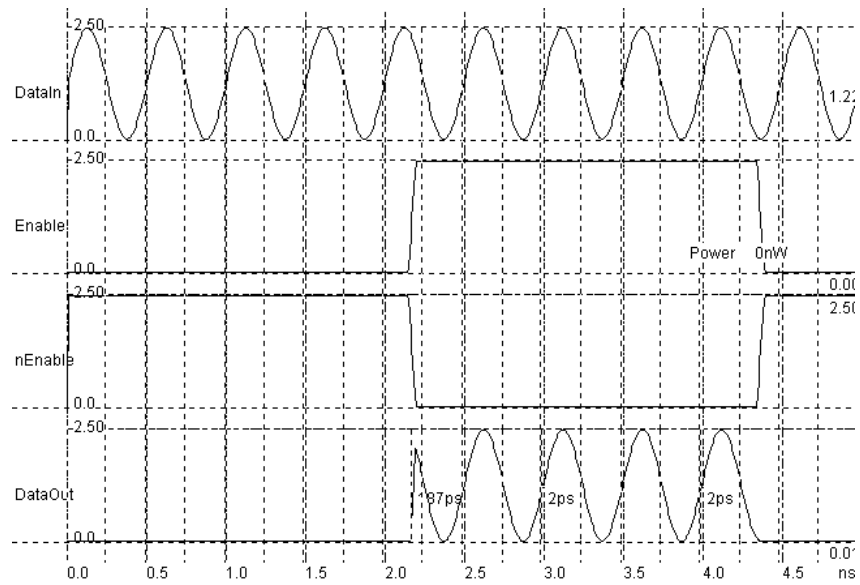


Fig. 2-34. Simulation of the transmission gate (TGATE.MSK)

EXERCISES

<To be added>