
11

Ultra deep submicron features

The technology scale down towards very narrow channels (i.e $0.18\mu\text{m}$ and below), introduces new features that are introduced in this chapter.

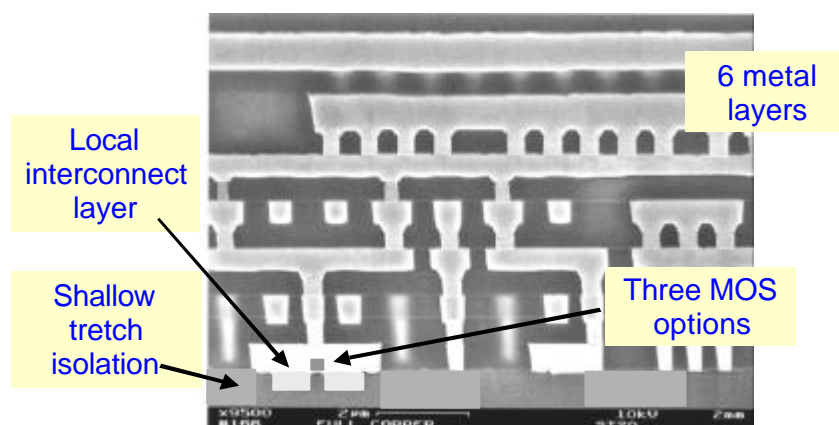


Fig. 11-xxx Ultra deep submicron features

Local Interconnect Layer (LIL)

A new layer is introduced for very short metal interconnections. The layer is called Local Interconnect Layer, or LIL.

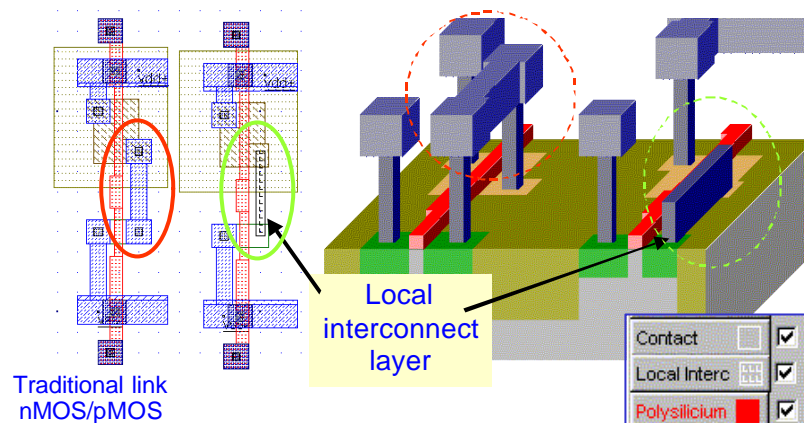


Fig. 11-xxx: Role of the local interconnect layer

Enable Local Interconnect Layer

Click "File" -> "Select Foundry" and choose "cmos018.rul". The LIL layer is now valid in the palette.

<Information on lateral LIL and contact>

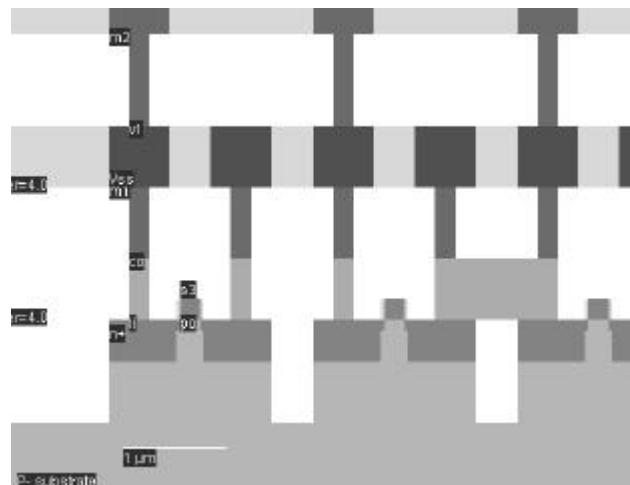


Fig. 11-xxx: Contacts

Low leakage MOS

A new kind of MOS device is introduced, called the low leakage MOS device. The main objective is to reduce significantly the I_{off} current, that is the small current that flows from between drain and source with a gate voltage 0 (Supposed to be no current in first order approximation). On the figure below, the low leakage MOS device (right side) has an I_{off} current reduced by a factor 50, thanks to a higher threshold voltage (0.45V rather than 0.35V).

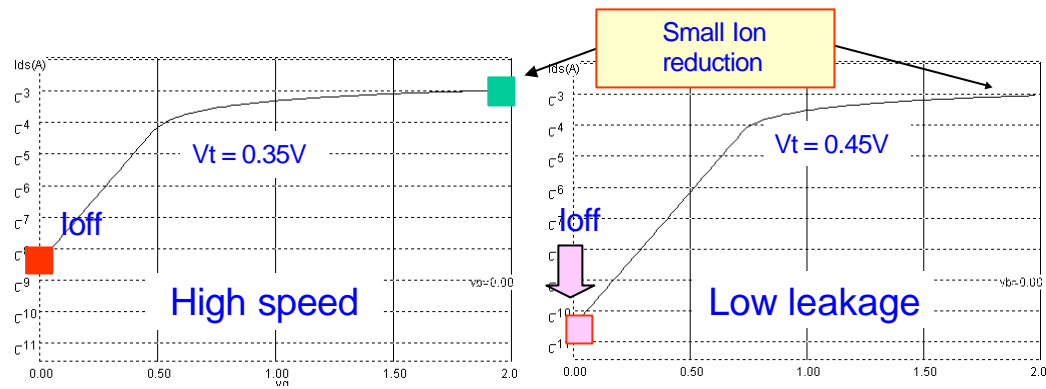


Fig. 11-xxx: Low leakage MOS for lower I_{off} current

<Example of standby current for a passive layout block>

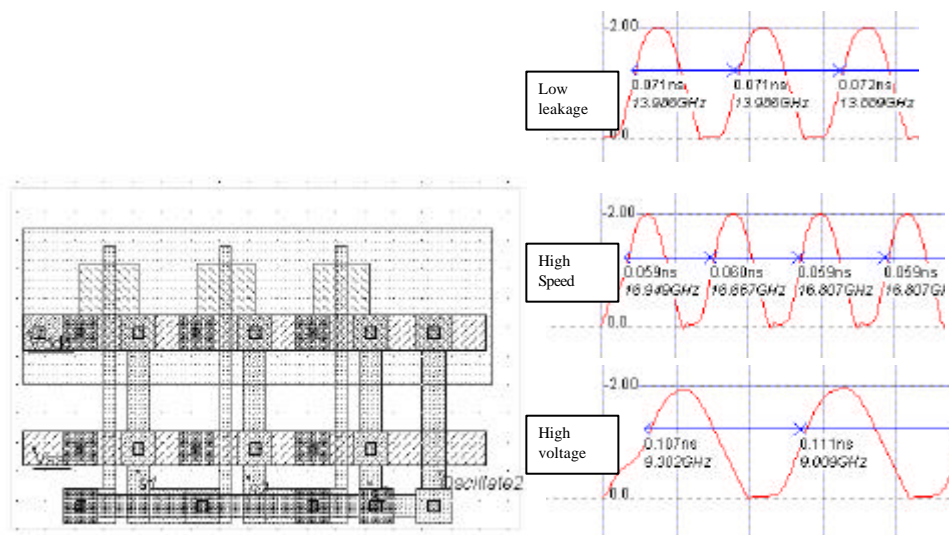


Fig. 11-xxx: Comparative simulation of the ring oscillator

Low inter-metal dielectric

New materials are introduced for dielectrics, in order to reduce the lateral parasitic coupling between interconnects. The material with low dielectric constant is called "Low K Silicon oxide", or SiOLK. The SiOLK permittivity should ideally be 1, that is corresponding to air. In reality, for 0.18 μm technology, SiOLK ϵ_r is around 3.0.

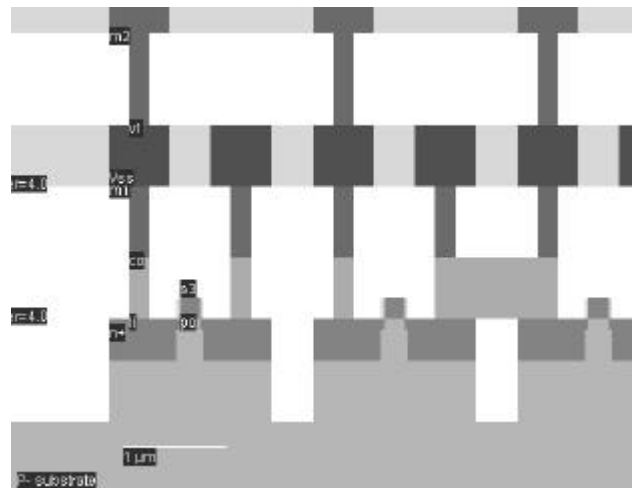


Fig. 11-xxx: Low dielectric permittivity between lateral metal interconnects reduces the crosstalk effect

<Demo on LowK reduction>