

A

Design Rules

This section gives information about the design rules used by Microwind2. You will find all the design rule values common to all CMOS processes. All that rules, as well as process parameters and analog simulation parameters are detailed here.

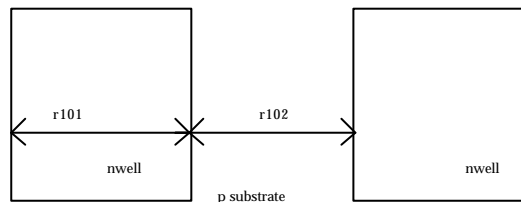
Design Rules

The software can handle various technologies. The process parameters are stored in files with the appendix '.RUL'. The default technology corresponds to a generic 6-metal 0.25 μ m CMOS process. The default file is CMOS025.RUL.

To select a new foundry, click on **File -> Select Foundry** and choose the appropriate technology in the list.

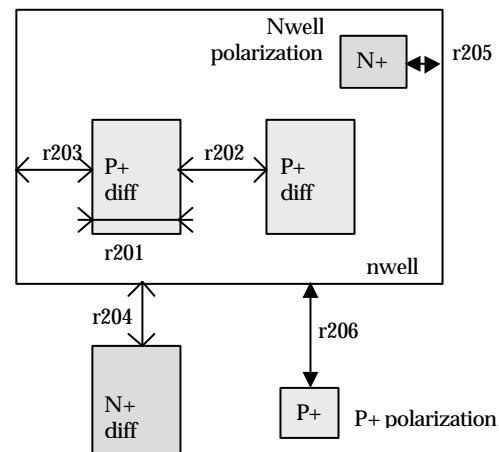
N-Well

- r101 Minimum well size : 12λ
- r102 Between wells : 12λ
- r110 Minimum surface : $144 \lambda^2$



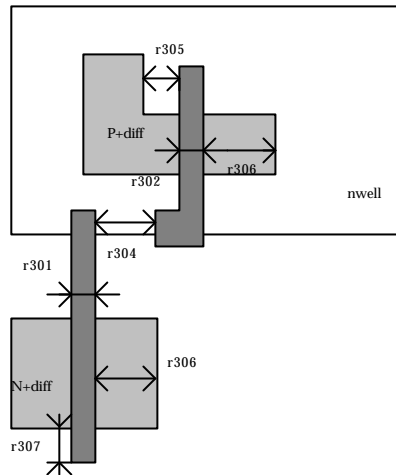
Diffusion

- r201 Minimum N+ and P+ diffusion width : 4λ
- r202 Between two P+ and N+ diffusions : 4λ
- r203 Extra nwell after P+ diffusion : 6λ
- r204 Between N+ diffusion and nwell : 6λ
- r205 Border of well after N+ polarization 2λ
- r206 Distance between Nwell and P+ polarization 6λ
- r210 Minimum surface : $24 \lambda^2$

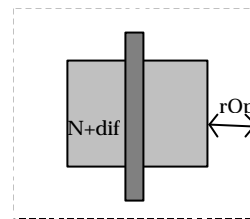


Polysilicon

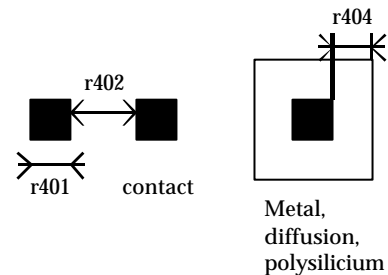
- r301 Polysilicon width : 2λ
- r302 Polysilicon gate on n+ diffusion: 2λ
- r303 Polysilicon gate on p+ diffusion: 2λ
- r304 Between two polysilicon boxes : 3λ
- r305 Polysilicon vs. other diffusion : 2λ
- r306 Diffusion after polysilicon : 4λ
- r307 Extra gate after polysilicium : 3λ
- r310 Minimum surface : $8 \lambda^2$

**MOS option**

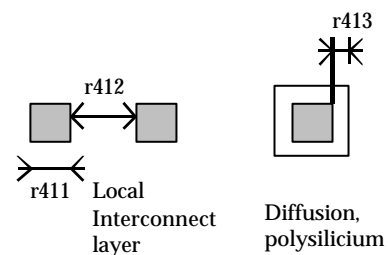
- rOpt Border of “option” layer over diff N+ and diff P+

**Contact**

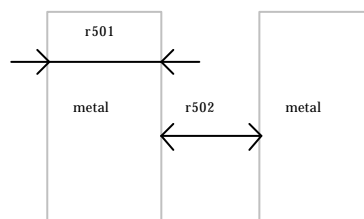
- r401 Contact width : 2λ
- r402 Between two contacts : 5λ
- r403 Extra diffusion over contact: 2λ
- r404 Extra poly over contact: 2λ
- r405 Extra metal over contact: 2λ

**Local Interconnect Layer (LIL, only starting 0.18μm)**

- r411 Lil width : 2λ
- r412 Between two LIL : 3λ
- r413 Extra diffusion, polysilicon over LIL: 1λ
- r420 Minimum surface : $8 \lambda^2$

**Metal 1**

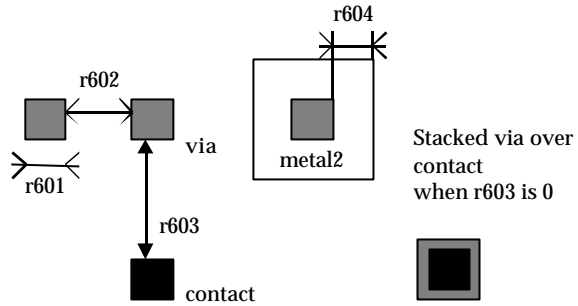
- r501 Metal width : 4λ
- r502 Between two metals : 4λ
- r510 Minimum surface : $32 \lambda^2$



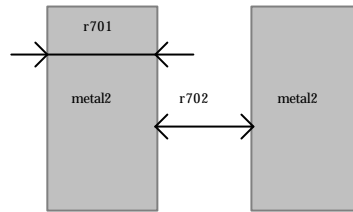
Via

- r601 Via width : 2λ
 r602 Between two Via: 5λ
 r603 Between Via and contact: 0λ
 r604 Extra metal over via: 2λ
 r605 Extra metal2 over via: 2λ

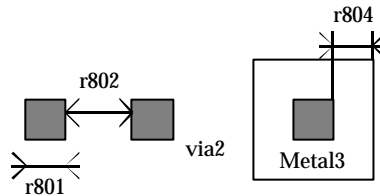
When $r603=0$, stacked via over contact is allowed

**Metal 2**

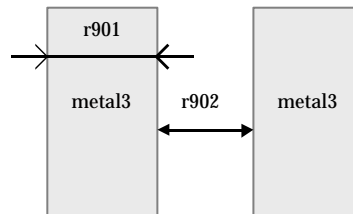
- r701 Metal width: 4λ
 r702 Between two metal2: 4λ
 r710 Minimum surface : $32 \lambda^2$

**Via 2**

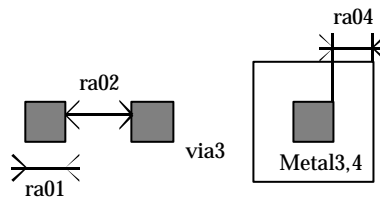
- r801 Via2 width : 2λ
 r802 Between two Via2: 5λ
 r804 Extra metal2 over via2: 2λ
 r805 Extra metal3 over via2: 2λ

**Metal 3**

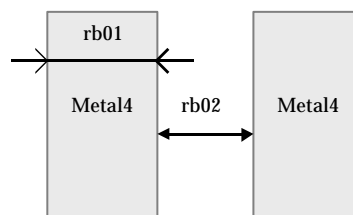
- r901 Metal3 width: 4λ
 r902 Between two metal3: 4λ
 r910 Minimum surface : $32 \lambda^2$

**Via 3**

- ra01 Via3 width : 2λ
 ra02 Between two Via3: 5λ
 ra04 Extra metal3 over via3: 2λ
 ra05 Extra metal4 over via3: 2λ

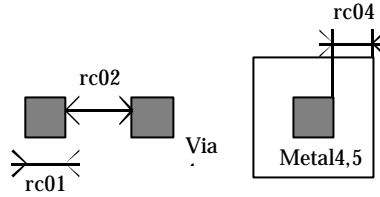
**Metal 4**

- rb01 Metal4 width: 4λ
 rb02 Between two metal4 : 4λ
 rb10 Minimum surface : $32 \lambda^2$

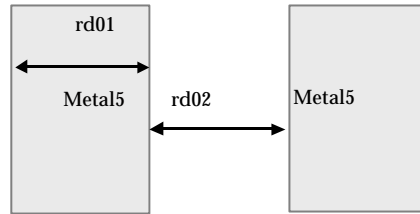


Via 4

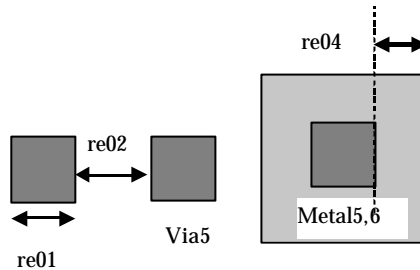
rc01	Via4 width : 2λ
rc02	Between two Via4: 5λ
rc04	Extra metal4 over via2: 3λ
rc05	Extra metal5 over via2: 3λ

**Metal 5**

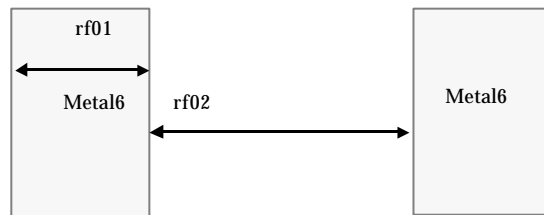
rd01	Metal5 width: 8λ
rd02	Between two metal5 : 8λ
rd10	Minimum surface : $100 \lambda^2$

**Via 5**

re01	Via5 width : 4λ
re02	Between two Via5: 6λ
re04	Extra metal5 over via5: 3λ
re05	Extra metal6 over via5: 3λ

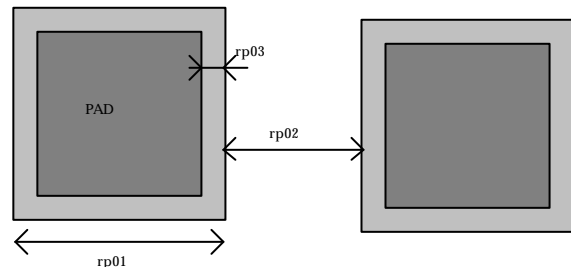
**Metal 6**

rf01	Metal6 width: 8λ
rf02	Between two metal6 : 15λ
rf10	Minimum surface : $300 \lambda^2$

**Pads**

The rules are presented below in μm . In .RUL files, the rules are given in lambda. As the pad size has an almost constant value in μm , each technology gives its own value in λ .

rp01	Pad width: $100 \mu\text{m}$
rp02	Between two pads $100 \mu\text{m}$
rp03	Opening in passivation v.s via : $5 \mu\text{m}$
rp04	Opening in passivation v.s metals: $5 \mu\text{m}$
rp05	Between pad and unrelated active area : $20 \mu\text{m}$



Parasitic Capacitors

Each deposited layer is separated from the substrate by a SiO₂ oxide and generated by a parasitic capacitor. The unit is the aF/μm² (atto = 10⁻¹⁸). Basically all layers generate parasitic capacitors. Diffused layers generate junction capacitors (N+/P-, P+/N). The list of capacitance handled by MICROWIND2 is given below. The name corresponds to the code name used in CMOS025.RUL (CMOS 0.25μm)

Surface capacitance refers to the body. Vertical crosstalk capacitance refer to inter-layer coupling capacitance, while lateral crosstalk capacitance refer to adjacent interconnects.

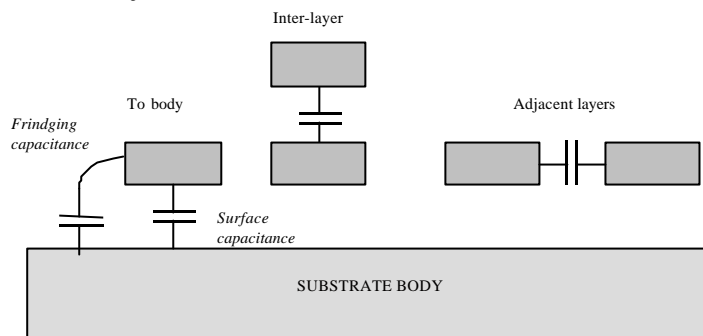


Figure A-1: Capacitances

SURFACE CAPACITANCE

NAME	DESCRIPTION	LINEIC (aF/μm)	SURFACE (aF/μm ²)
CpoOxyde	Polysilicon/Thin oxide capacitance	n.c	4600
CpoBody	Polysilicon to substrate capacitance	n.c	80
CMEBody	Metal on thick oxide to substrate	42	28
CM2Body	Metal2 on body	36	13
CM3Body	Metal3 on body	33	10
CM4Body	Metal4 on body	30	6
CM5Body	Metal5 on body	30	5
CM6Body	Metal6 on body	30	4

INTER-LAYER CROSSTALK CAPACITANCE

NAME	DESCRIPTION	VALUE (aF/μm ²)
CM2Me	Metal2 on metal 1	50
CM3M2	Metal3 on metal 2	50
CM4M3	Metal4 on metal 3	50
CM5M4	Metal5 on metal 4	50
CM6M5	Metal6 on metal 5	50

LATERAL CROSSTALK CAPACITANCE

NAME	DESCRIPTION	VALUE (aF/μm)
CMeMe	Metal to metal (at 4λ distance, 4λ width)	10
CM2M2	Metal2 to metal 2	10
CM3M3	Metal3 to metal 3	10
CM4M4	Metal4 to metal 4	10
CM5M5	Metal5 to metal 5	10
CM6M6	Metal6 to metal6	10

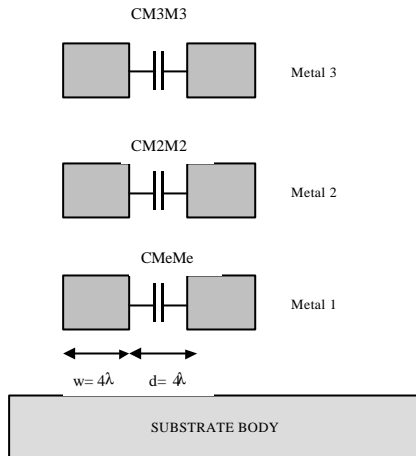


Figure A-2: Crosstalk capacitance

The crosstalk capacitance value per unit length is given in the design rule file for a predefined interconnect width ($w=4\lambda$) and spacing ($d=4\lambda$).

In Microwind2,

- The computed crosstalk capacitance is not dependant on the interconnect width w .
- The computed crosstalk capacitance value is proportional to $1/d$ where d is the distance between interconnects.

Vertical Aspect of the Technology

The vertical aspect of the layers for a given technology is described in the RUL file after the design rules, using coed HE (height) and TH (thickness) for all layers. The figure A-3 below illustrates the altitude 0, which corresponds to the channel of the MOS. The height of diffused layers can be negative, for P++ EPI layer for example.

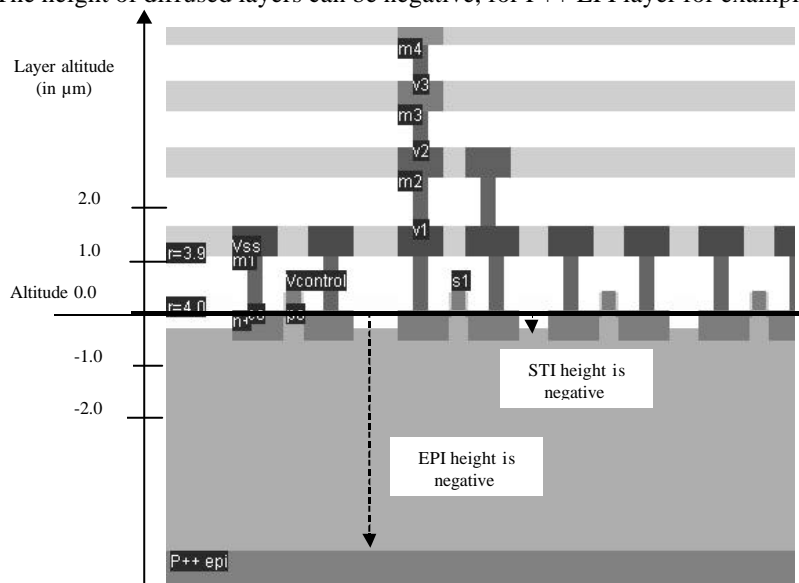


Figure A-2: Description of the 2D aspect of the CMOS technology

LAYER	DESCRIPTION	PARAMETERS
EPI	Buried layer made of P++ used to create a good ground reference underneath the active area.	HEEPI for height (negative in respect to the origin) THEPI for thickness
STI	Shallow trench isolation used to separate the active areas.	HESTI for height THSTI for thickness
PASSIVATION	Upper SiO2 oxide on the top of the last metal layer	HEPASS for height THPASS for thickness
NITRIDE	Final oxide on the top of the passivation, usually Si3N4.	HENIT for height THNIT for thickness
NISO	Buried N- layer to isolate the Pwell underneath the nMOS devices, to enable forward bias and back bias	HENBURRIED for height THNBURRIED for thickness

Simulation Parameters

The following list of parameters is used in Microwind2 to configure the simulation.

CODE	DESCRIPTION	TYPICAL VALUE
VDD	Supply voltage of the chip	2.0 V
HVDD	High voltage supply	3.3V
DELTAT	Simulator minimum time step to ensure convergence. You may increase this value to speed up the simulation but instability problems may rise.	0.5e-12 s
TEMPERATURE	Operating temperature of the chip	25 °C

MOS MODEL 3 PARAMETERS			
PARAMETER	DEFINITION	TYPICAL VALUE 0.25μm	
		NMOS	pMOS
L3VTO	Threshold voltage	0.4V	-0.4V
L3KP	Transconductance coefficient	300μA/V ²	120μA/V ²
L3PHI	Surface potential at strong inversion	0.3V	0.3V
L3LD	Lateral diffusion into channel	0.01μm	0.01μm
L3GAMMA	Bulk threshold parameter	0.4 V ^{0.5}	0.4 V ^{0.5}
L3KAPPA	Saturation field factor	0.01 V ¹	0.01 V ¹
L3VMAX	Maximum drift velocity	150Km/s	100Km/s
L3THETA	Mobility degradation factor	0.3 V ¹	0.3 V ¹
L3NSS	Subthreshold factor	0.07 V ¹	0.07 V ¹

L3V2TO	Threshold voltage of low leakage MOS	0.6V	-0.6V
L3K2P	Transconductance coefficient of high voltage MOS	150μA/V ²	80μA/V ²

Ultra deep submicron features

Some options are built in Microwind2 to enable specific features of ultra deep submicron technology. Details are provided in the table below.

CODE	DESCRIPTION	VALUE
LOWK	Inter-metal oxide with reduced permittivity to reduce later cross-talk	3.0
LIL	Local interconnect layer	1 = enable, 0 = disable
NISO	Buried nwell layer to enable full isolation of the pwell region underneath nMOS devices	1 = enable, 0 = disable
TOX	Normal MOS gate oxide thickness	0.004 μm (40 Å)
HVTOX	High voltage gate oxide thickness	0.007 μm (70 Å)
SALICIDE	Specific layer to reduce surface resistance, thus reducing N+,P+ and polysilicon resistance by a factor 10	1 = enable, 0 = disable

Design Rule File

An example of design rule file corresponding to a CMOS 0.18 μ m technology is given below.


```

MICROWIND 2.0
*
* Rule File for CMOS 0.18µm
* Date : 18 May 98 by Etienne Sicard
* Date : 27 April 99 By Etienne/Fabrice
* 16 May 99 r603 dist via/contact
* 23 Jun 99 KOR mm9
* 04 Jan 00 smaller dT
* 19 Feb 00 STI, Niso, LL, high VT,
LIL
*
* status : preliminary
*
NAME CMOS 0.18µm - 6 Metal
*
lambda = 0.1      (Lambda is set to half the
gate size)
metalLayers = 6   (Number of metal layers :
6)
lowK = 4.0        (inter-metal oxide)
lil = 1           (local interconnect layer
l=enable, 0= disable)
tox = 0.004       (fast MOS oxide in µm
0.0=disable)
hytox= 0.007      (high voltage MOS oxide)
salicide = 0      (Enable salicide l=enable
0= disable)
*
* Design rules associated to each layer
*
* Well (Gds2 level 1)
r101 = 10         (well width)
r102 = 11         (well spacing)
*
* Diffusion (N+ 16, P+ 17, active 2)
*
r201 = 4          (diffusion width)
r202 = 4          (diffusion spacing)
r203 = 6          (border of nwell on diffp)
r204 = 6          (nwell to next diffn)
*
* Poly (13)
*
r301 = 2          (poly width)
r302 = 2          (ngate width)
r303 = 2          (pgate width)
r304 = 3          (poly spacing)
r305 = 1          (spacing poly and unrelated
diff)
r306 = 4          (width of drain and source
diff)
r307 = 2          (extra gate poly)
* Contact (19)
r401 = 2          (contact width)
r402 = 3          (contact spacing)
r403 = 2          (metal border for contact)
r404 = 2          (poly border for contact)
r405 = 2          (diff border for contact)
* metal (23)
r501 = 3          (metal width)
r502 = 4          (metal spacing)
* via (25)
r601 = 3          (Via width)
r602 = 4          (Spacing)
r603 = 0          (via/contact)
r604 = 2          (border of metal&metal2)
* metal 2 (27)
r701 = 3          (Metal 2 width)
r702 = 4          (spacing)
* via 2 (32)
r801 = 3          (Via width)
r802 = 4          (Spacing)
r804 = 2          (border of metal2&metal3)
* metal 3 (34)
r901 = 3          (width)
r902 = 4          (spacing)
* via 3 (35)
ra01 = 3          (Via width)
ra02 = 4          (Spacing)
ra04 = 2          (border of metal3&metal4)
* metal 4 (36)
rb01 = 3          (width)
rb02 = 4          (spacing)
* via 4 (52)
rc01 = 3          (Via width)
rc02 = 4          (Spacing)
rc04 = 2          (border of metal4&metal5)

```

```

* metal 5 (53)
rd01 = 8          (width)
rd02 = 8          (spacing)
* via 5 (xx)
re01 = 5          (Via width)
re02 = 5          (Spacing)
re04 = 2          (border of metal5&metal6)
* metal 6 (xx)
rd01 = 8          (width)
rd02 = 15         (spacing)
*
* Passivation nitride (31) and pad rules
*
rp01 = 800        (Pad width)
rp02 = 800        (Pad spacing)
rp03 = 40         (Border of Vias)
rp04 = 40         (Border of metals)
rp05 = 200        (to unrelated active areas)
*
* Option layer around MOS
*
ropt = 5
*
* Thickness of conductors for process
aspect
* All in µm
*
* P++ epitaxial
thepe = 1.0
heepi = -4.0
* niso description
thnburried = 1.0
henburried = -3.0
* Shallow trench isolation
thsti = 1.0
hesti = -1.0
* Poly
thpoly = 0.20
hepoly = 0.01
* Local interconnect
thlil = 0.6
helil = 0.0
* contact
thco = 0.7
heco = 0.5
thdn = 0.4
thdp = 0.4
thnw = 2.0
thme = 0.6
heme = 1.3
thm2 = 0.6
hem2 = 2.8
thm3 = 0.6
hem3 = 4.4
thm4 = 0.6
hem4 = 6.1
thm5 = 1.0
hem5 = 7.7
thm6 = 1.0
hem6 = 9.6
* Passivation
thpass = 0.5
hepass = 10.6
* Nitride
thnit = 0.6
henit = 11.2
*
* Resistances Copper
* Unit is ohm/square
*
repo = 4
reco = 2
reli = 0.25
reme = 0.15
revi = 1
rem2 = 0.06
rev2 = 2
rem3 = 0.06
rev3 = 23
rem4 = 0.06
rev4 = 1
rem5 = 0.03
rev5 = 1
rem6 = 0.03
*
* Parasitic capacitances

```

```

*
cpoOxyde= 4600 (Surface capacitance
Poly/Thin oxyde aF/μm2)
cpobody = 80 (Poly/Body)
clibody = 40
clibody = 40
cmebody = 28
cmelineic = 42
cmepoly = 60
cm2body = 20
cm2lineic = 30
cm2metal = 38
cm3body = 20
cm3lineic = 30
cm4body = 20
cm4lineic = 30
cm5body = 20
cm5lineic = 40
cm6body = 20
cm6lineic = 40
cgsn = 500 ( Gate/source capa of
nMOS)
cgsp = 500
*
* Vertical crosstalk
*
cm2me = 50
cm3m2 = 50
cm4m3 = 50
cm5m4 = 50
cm6m5 = 50
*
* Lateral Crosstalk
*
cmextk = 10 (Lineic capacitance for
crosstalk coupling in aF/μm)
cm2xtk = 12 (C is computed using
Cx=cmextk*1/spacing)
cm3xtk = 12
cm4xtk = 12
cm5xtk = 12
cm6xtk = 12
*
* Junction capacitances
*
cdnpwell = 350 (n+/psub)
cdpnwell = 300 (p+/nwell)
cnwell = 250 (nwell/psub)
cpwell = 100 (pwell/nsup)
cldn = 100 (Lineic capacitance N+/P-
aF/μm)
cldp = 100 (Idem for P+/N-)
*
* Nmos Model 3 parameters
*
NMOS
l3vto = 0.40
l3vmax = 130e3
l3gamma = 0.4
l3theta = 0.3
l3kappa = 0.01
l3phi = 0.2
l3ld = 0.01
l3kp = 400e-6
l3nss = 0.07
* High voltage
l3k2p = 200e-6
* Low leakage
l3v2to = 0.6
*
* Pmos Model 3
*
PMOS
l3vto = -0.40
l3vmax = 100e3
l3gamma = 0.4
l3theta = 0.3
l3kappa = 0.01
l3phi = 0.2
l3ld = 0.01
l3kp = 150e-6
l3nss = 0.07
* High voltage
l3k2p = 75e-6
* Low leakage
l3v2to = -0.6
*

```

```

* MM9 Model parameters
*
* Nmos MM9
*
NMOS
vto = 0.40
v2to = 0.6
slvto = 0.01e-6
swvto = 0.0e-6
lap = 0.021e-6
wot = 0.033e-6
kor = 0.25
slko = -0.07e-6
swko = 0.05e-6
ler = 10e-6
wer = 10e-6
phib = 0.65
betsq = 400e-6
zet1 = 0.35
mor = 0.368
gamo = 0.010
slgamo = 0e-6
gam1 = 0.034
slgam1 = -0.5e-6
swgam1 = 0.05e-6
thel = 0.12
slthel = 0.10e-6
swthel = 0.00e-6
the2 = 0.13
slthe2 = -0.02e-6
swthe2 = 0.06e-6
the3 = 0.06
slthe3 = 0.06e-6
swthe3 = -0.08e-6
vsbtr = 0.156
vsbtr = 2.0
*
* Pmos MM9
*
PMOS
vto = 0.40
v2to = 0.6
slvto = 0.0
swvto = 0.0
lap = 0.017e-6
wot = 4.5e-8
kor = 0.25
slko = -3.2e-8
swko = 7.6e-9
ler = 10e-6
wer = 10e-6
betsq = 160e-6
zet1 = 1.43
mor = 0.33
phib = 0.65
gamo = 0.010
slgamo = 2.6e-15
gam1 = 0.045
slgam1 = -0.1e-6
swgam1 = 0.0
thel = 0.44
slthel = 0.072e-6
swthel = -5e-8
the2 = 0.25
slthe2 = -3.67e-8
swthe2 = 3.0e-8
the3 = 0.002
slthe3 = 0.43e-8
swthe3 = 2.0e-8
vsbtr = 0.156
vsbtr = 0.073
*
* CIF & Gds2 Layers
* MicroWind layer, CIF layer, Gds2 layer,
overetch
*
cif nwell 1 1 0.0
cif diffp 17 17 0.5
cif diffn 16 16 0.5
cif aarea 2 2 0.5
cif poly 13 13 0.0
cif lil 14 14 0.0
cif contact 19 19 0.025
cif metal 23 23 0.0125
cif via 25 25 0.0125
cif metal2 27 27 0.0125
cif via2 32 32 0.0125

```

```
cif metal3 24 34 0.0125
cif via3 35 35 0.0125
cif metal4 36 36 0.0125
cif via4 52 52 0.0125
cif metal5 53 53 0.0
cif via5 54 54 0.0
cif metal6 55 55 0.0
cif passiv 31 31 0.0
cif option 40 40 0.0
cif text 56 56 0.0
*
*
* MicroWind simulation parameters
*
deltaT = 0.5e-12 (Minimum simulation
interval dT)
vdd = 2.0
temperature = 27
*
* End CMOS 0.18 µm
```