

9

Interconnects

Introduction

The role of interconnects in integrated circuit performances has considerably increased with the technology scale down. Figure 9-1 shows the evolution of the aspect of the integrated circuit. In 0.18 μm , 6 metal layers are available. The capacitance effects have severely increased due to much nearer routing, and the interconnect resistance has significantly increased due to a continuous reduction of the wire section.

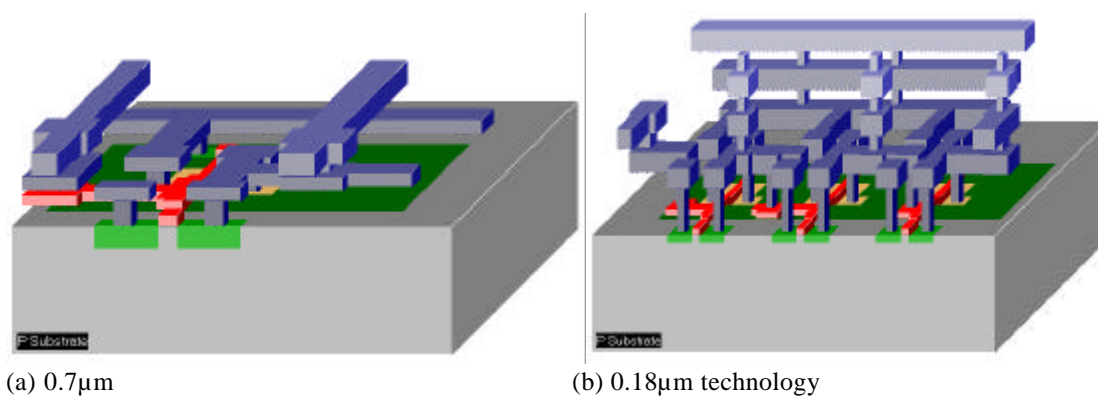


Figure 9-1: Evolution of interconnect between 0.7 μm technology and 0.18 μm technology

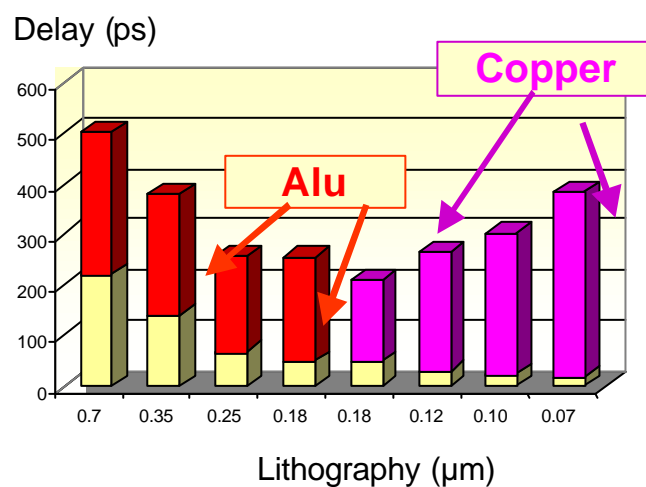


Figure 9-2: Evolution of interconnect delay with the technology scale down

The consequence is that the RC delay provoked by the interconnect is becoming predominant and can be considered as the main limiting factor in terms of operating frequency within the integrated circuit. In figure 9-2, the evolution of a “typical” propagation delay within an interconnect is computed with varying technologies, from $0.8\mu\text{m}$ down to $0.1\mu\text{m}$. It can be seen that

- ♦ the gate delay is still significant in $0.7\mu\text{m}$
- ♦ the interconnect delay increases significantly in $0.18\mu\text{m}$
- ♦ the introduction of low resistivity materials such as copper induces some gain
- ♦ the continuous scale down increases the interconnect delay

Interconnect parameters

Some details about the size and electrical properties of the interconnects are reported in figure 9-3. The metal pitch is following the lithography, but the interconnect thickness is not reduced with the same trend. The cross-section of the interconnect is reduced, leading to a higher resistance per length unit. Starting at $0.18\mu\text{m}$, aluminum is replaced by copper which has a lower resistivity.

Technology	Metal layers	Lower metal Pitch (μm)	Upper metal Pitch (μm)	Thickness metal (μm)	Resistance (Ω/sq)	Interconnect Materials	Microwind2 file
$1.2\mu\text{m}$	2	1.8	2.4	1.2	0.025	Alu, SiO ₂	cmos12.rul
$0.7\mu\text{m}$	2	1.2	1.6	1.1	0.025	Alu, SiO ₂	cmos07.rul
$0.5\mu\text{m}$	3	0.75	1.25	1.0	0.04	Alu, SiO ₂	cmos05.rul
$0.35\mu\text{m}$	5	0.6	1.2	1.0	0.05	Tu, Alu, SiO ₂	cmos035.rul
$0.25\mu\text{m}$	6	0.45	0.9	0.9	0.07	Tu, Alu, SiO ₂	cmos025.rul
$0.18\mu\text{m}$	6	0.3	0.6	0.8	0.07	Tu, Cu, SiO ₂	cmos018.rul
$0.12\mu\text{m}$	7	0.22	0.5	0.7	0.06	Tu, Cu, SiO ₂	cmos012.rul

Figure 9-3: Evolution of interconnect parameters with the technology scale down

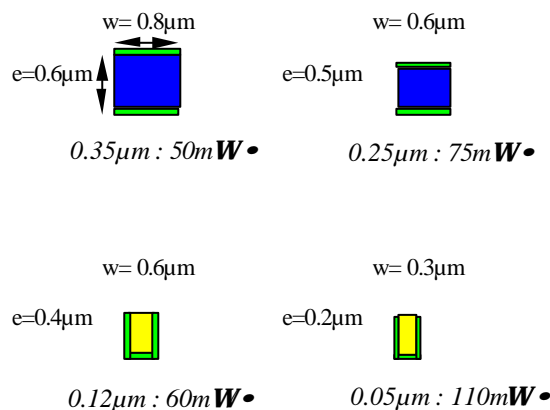


Figure 9-4: Evolution of interconnect resistance with the technology scale down

Delay within interconnects

The delay within interconnects is handled in Microwind2 as follows. Consider the circuit Rceffect.MSK, shown figure 9-5. It represents a buffer (Left upper corner), which drives a long interconnect, and then a loading inverter.

Although both the capacitance and resistance of each node are extracted, the simulator considers by default only the capacitance and ignores the resistance. We add a “virtual” resistance using the resistance icon situated in the palette. This resistance is placed as detailed below, to create two separate nodes. We fix manually the value of the resistance, here $1000\ \Omega$.

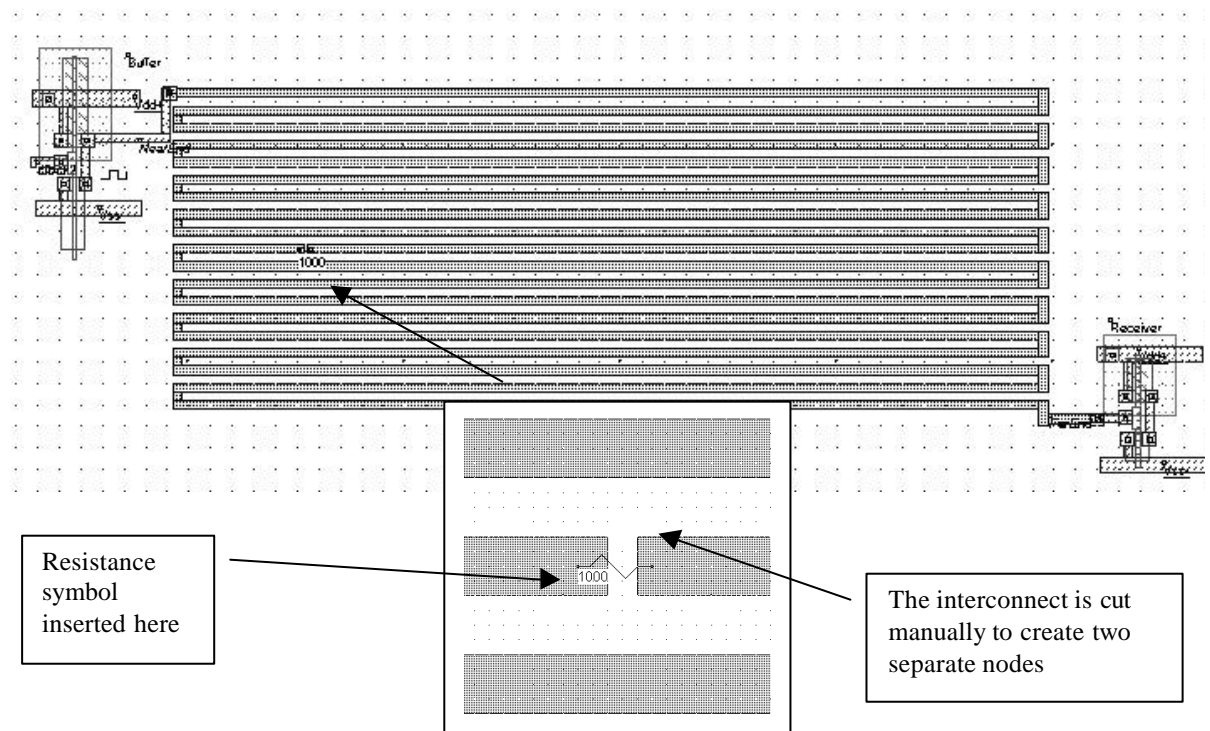


Figure 9-5 : adding a virtual resistance within the layout to simulate the resistance.

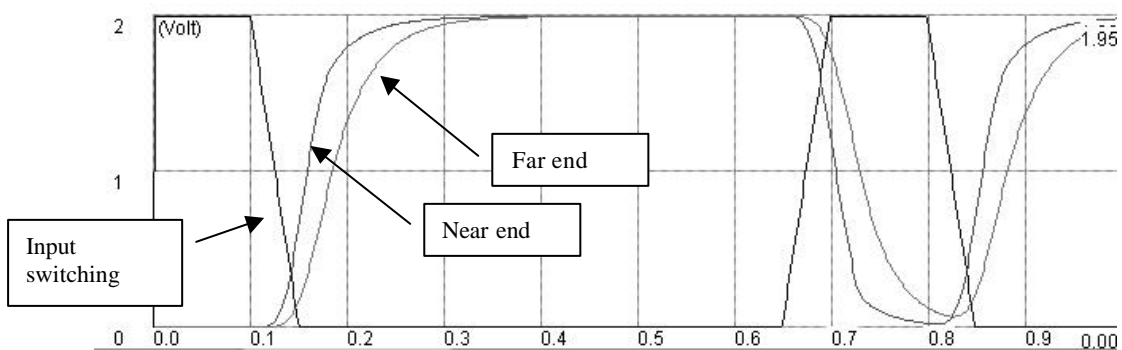


Figure 9-6 : RC delay simulation (RCEffect.MSK).

Global Delay Computing

At integrated circuit level, there exist a possibility to evaluate the delay of each interconnect, in a global way, thanks to analytical approximations. We implemented in Microwind2 very simple approximations of the delay within interconnects, using the following formulations.

$$\text{delay} = 0.43 \cdot R_{\text{line}} \cdot C_{\text{line}} + 0.92 \cdot (R_{\text{line}} \cdot C_{\text{gate}} + R_{\text{d_mos}} \cdot (C_{\text{line}} + C_{\text{gate}}))$$

with

delay = RC delay of the propagation, in s

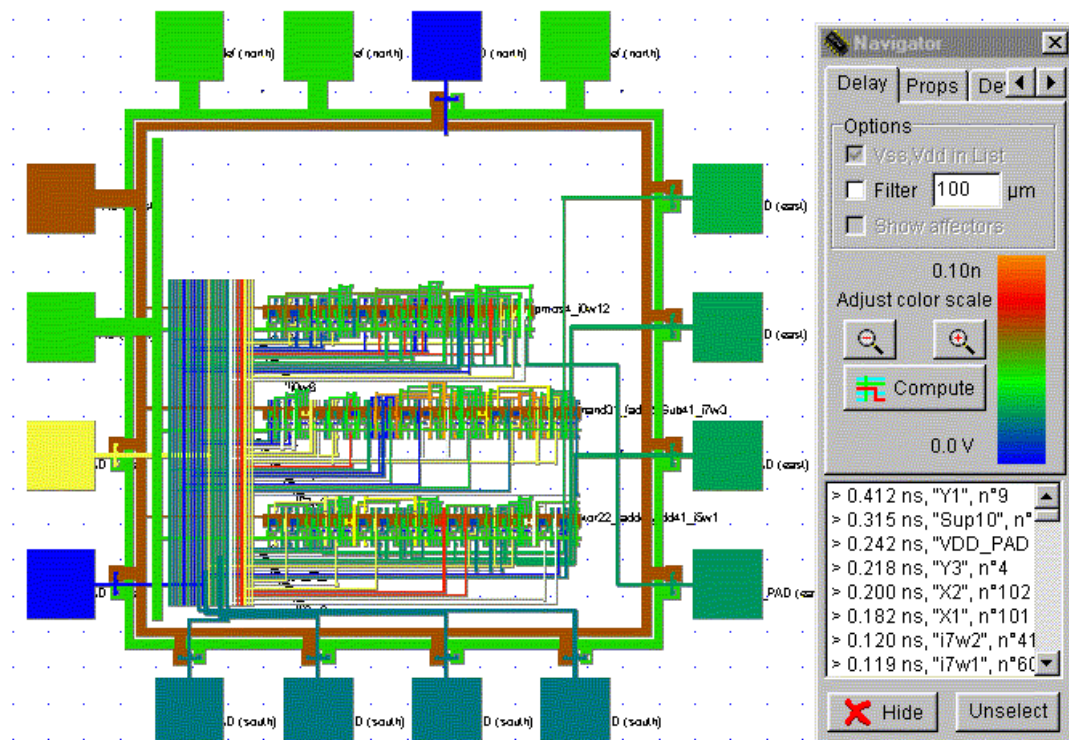
Rline= resistance of the line (in ohm)

Cline = capacitance of the interconnect (in Farad)

Cgate = capacitance of the loading gates (in Farad)

Rd_mos = equivalent on resistance of the MOS device driving the interconnect

Click “Analysis” -> “Global Delay analysis” within microwind2 to access to this command. The example of the complete delay calculation of each interconnect is displayed in figure 9-7. The classification of each nodes by decreasing delay appears in the navigator window. The worst delay appears at node Y1, with a delay estimated to 412 ps.



Crosstalk

Crosstalk is a parasitic effect that affects long lines routed close from each other. The demonstration of crosstalk can be made with the circuit CrosstalkBig.MSK, partially shown in figure 9-8. The schematic diagram of the circuit corresponds to two strong inverters, and strongly coupled interconnects. We used one interconnect “victim” fixed to Vss, surrounded by two aggressors which are switching, to exhibit the crosstalk effect. The proximity of the interconnects creates a coupling effect (C_{12} in the cross-section) that provokes crosstalk between the aggressor and victims.

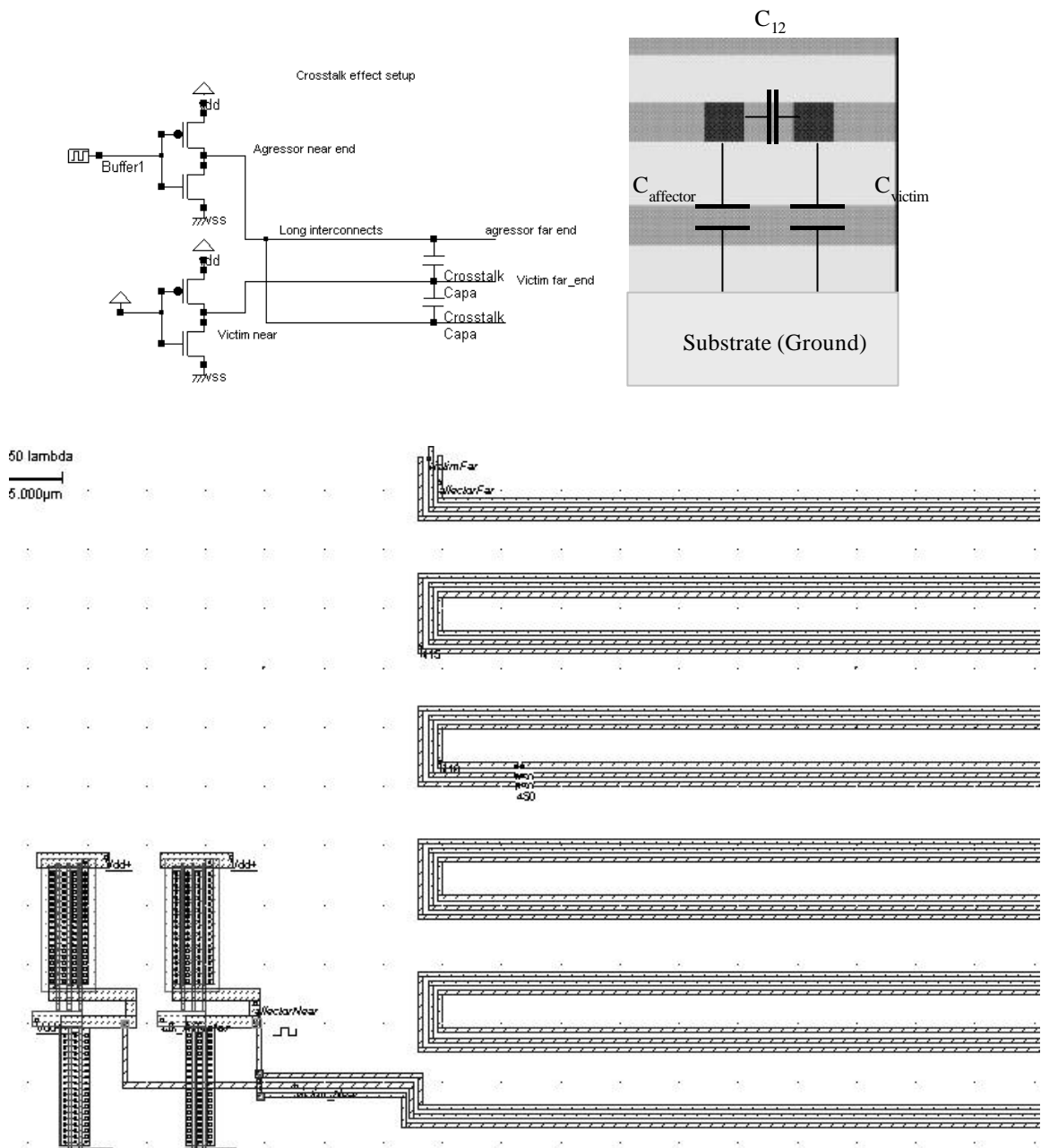


Figure 9-8 : Two buffers and coupled interconnects to exhibit the crosstalk effect (CrosstalkBig.MSK)

When you click “Simulate” “Start simulation”, you see no crosstalk effect on “Victim Far” and “Victim Near”. This is normal because the analog simulator do not consider the crosstalk capacitance by default. You must choose the command “Simulate” -> “With crosstalk”.

Click “Evaluate Min/max” and select “Victim Far” to compute on the screen the maximum amplitude of the crosstalk.

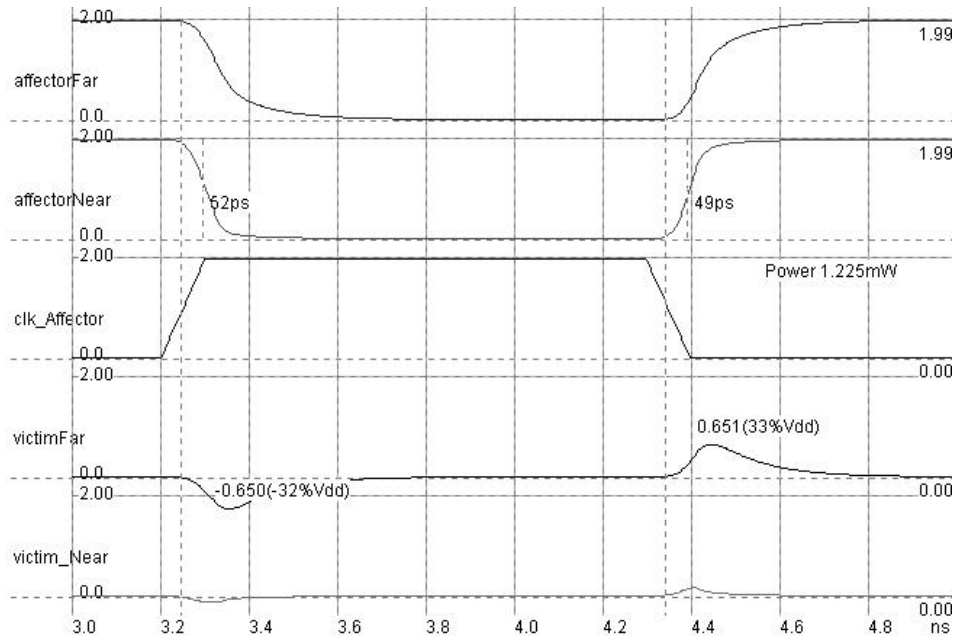


Figure 9-9: The crosstalk effect appearing in interconnects routed very close (CrosstalkBig.MSK)

Global Crosstalk

An evaluation of the crosstalk effect based on analytical approximations of the coupling amplitude is available within Microwind2. Click “Analysis” -> “Global Crosstalk analysis” to access to this command. The example of the complete crosstalk calculation of each interconnect is displayed in figure 9-10. The formulations used for the computation of the crosstalk voltage ΔV are shown below.

$$C_x = \frac{C_{12}}{C_{victim}}$$

$$x = \frac{W_{victim}}{L_{victim}} \frac{L_{affector}}{W_{affector}}$$

$$\Delta V = V_{dd} \frac{C_x}{1 + C_x} \frac{1}{1 + x}$$

With

C_{12} = crosstalk capacitance (Farad)

C_{victim} = capacitance of victim (Farad)

W = width of MOS device (m)

L = length of MOS device (m)

V_{dd} = supply voltage (V)

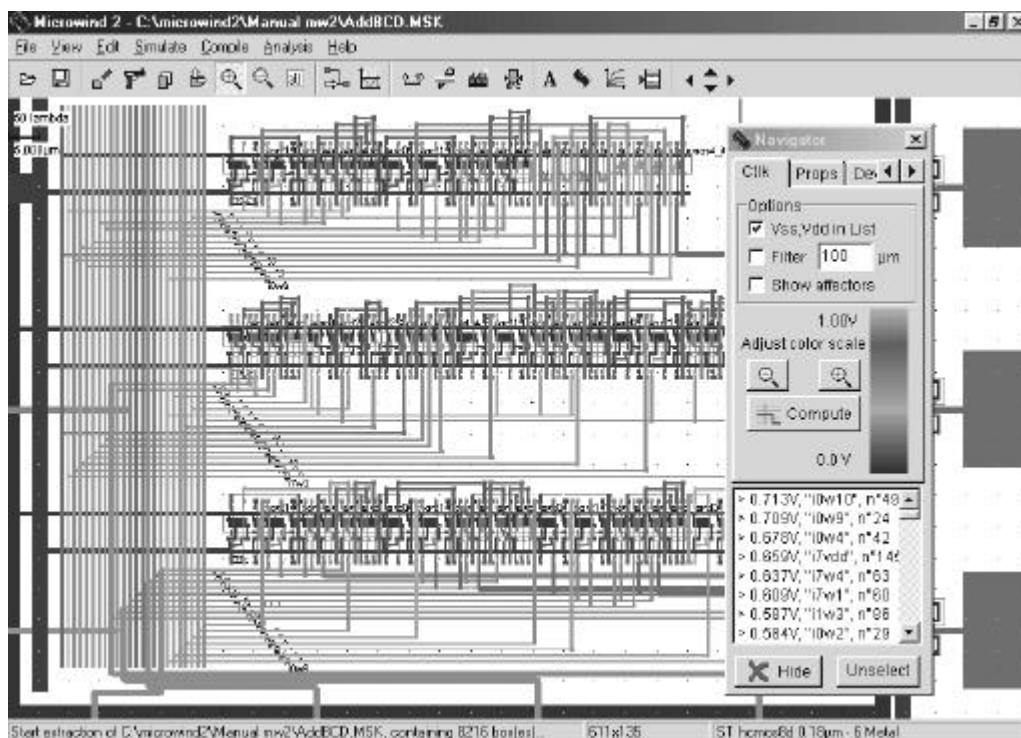
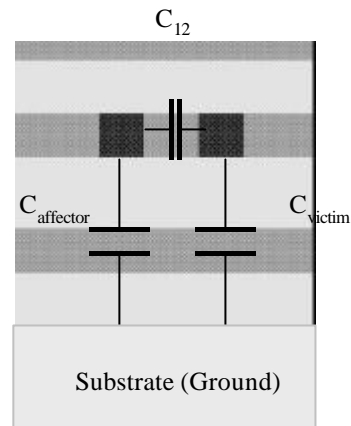


Figure 9-10: Global crosstalk extraction and classification of dangerous nodes (AddBCD.MSK)

Crosstalk in Sample/Hold circuits

An illustration of the crosstalk effect can be performed on the sample and hold circuit based on a transmission gate. Without considering the crosstalk effect, the simulation of a sinusoidal wave sampling leads to a "normal" behavior as shown in figure 9-11. With the option "Simulate with crosstalk", the simulation exhibits a small distortion of the sampled information, due to a capacitance coupling between the storage capacitance and the input.

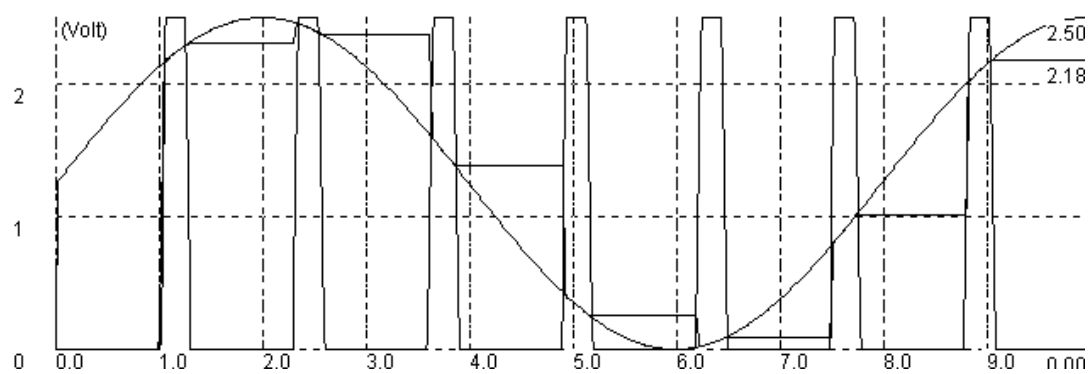


Figure 9-11: Sample-and-hold circuit without considering crosstalk (SampleHold.MSK)

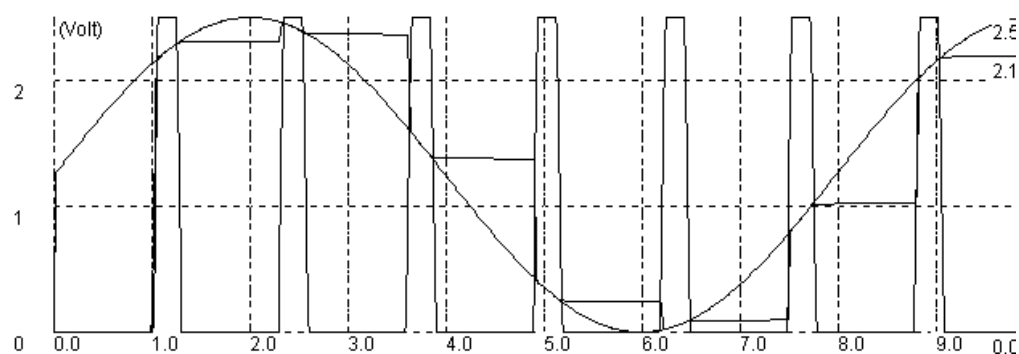


Figure 9-12: Sample-and-hold circuit when considering crosstalk (SampleHold.MSK)