

# 7

## Analog Cells

### Diode-connected MOS

The schematic diagram of the diode-connected MOS is proposed in figure 7-1. The question rises: is this device a capacitance, a diode or a resistance? The answer is: a capacitance for  $V_k < V_t$ , a diode with an interesting high resistance when  $V_k > V_t$ , where  $V_t$  is the threshold voltage of the device. The main application of this circuit is the design of a big resistance in a very small silicon area.

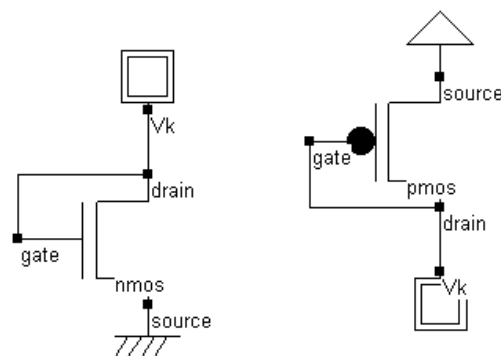


Figure 7-1 : MOS connected as a diode

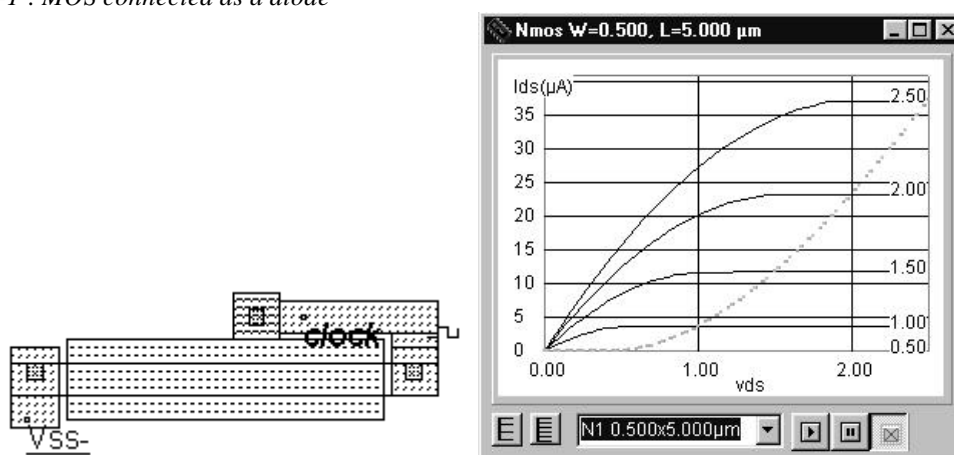
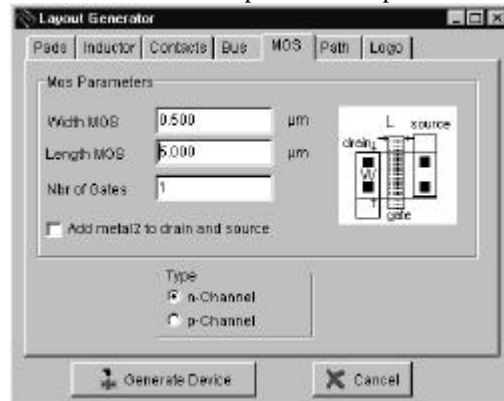


Figure 7-2 : Layout and simulation of the MOS connected as a diode

#### OPERATION



- ❶ In the palette, click the icon “MOS generator”.
- ❷ Enter a large length and a small width. For example, enter  $W=0.5\mu\text{m}$ ,  $L=5\mu\text{m}$ . This sizing corresponds to a long and narrow channel, featuring a very high resistance channel with poor current performances.



- ❸ Add a poly/metal contact and connect the gate to one diffusion. Add a clock on that node. Add a VSS property to the other diffusion.



- ❹ Click **Simulation on Layout**. In a small window, the MOS characteristics are drawn, with the functional point drawn as a color dot (Figure 7-2). It can be seen that the I/V characteristics correspond to a diode. The resistance varies with  $V_k$  but can be estimated around  $30\text{K}\Omega$ )

The resistance obtained using such a circuit can reach easily  $100\text{K}\Omega$  in a very small silicon area. The same resistance can be drawn in poly but would require a much larger area. In figure 7-3, a polysilicon resistance of  $20\text{K}\Omega$  is drawn close to the MOS device with a  $30\text{K}\Omega$  on resistance. The advantage of using MOS resistance rather than polysilicon resistance are obvious.

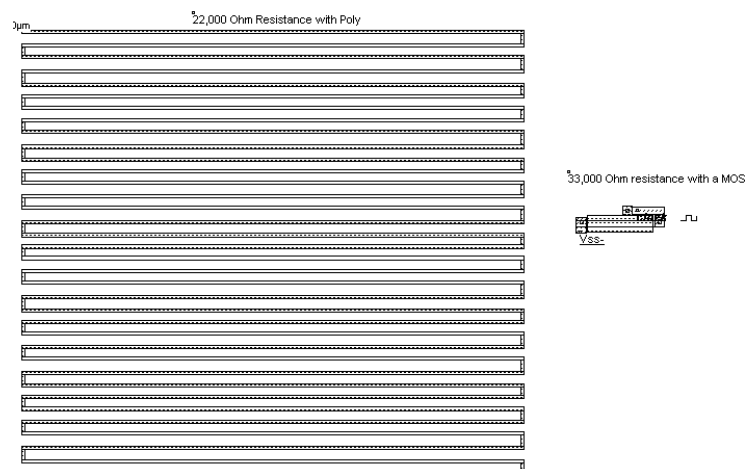


Figure 7-3 : A MOS device resistance compared to the same resistance in Poly(MosRes.MSK)

## Voltage Reference

The voltage reference is usually derived from a voltage divider made from resistance. The main problem is that the value of the resistance must be high to keep the short cut current low, to avoid wasted power consumption. A key idea is to use MOS devices rather than polysilicon or diffusion resistance to keep silicon area very small.

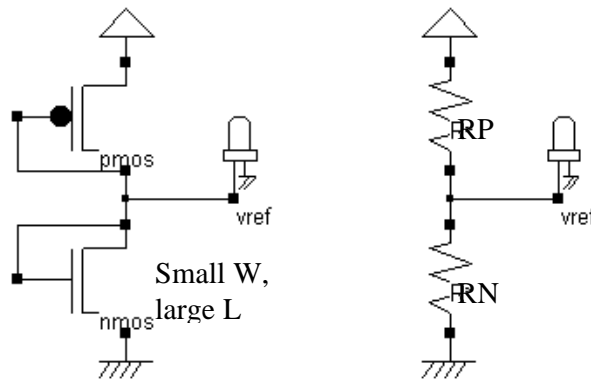


Figure 7-4 : Voltage reference using PMOS and NMOS devices as large resistance

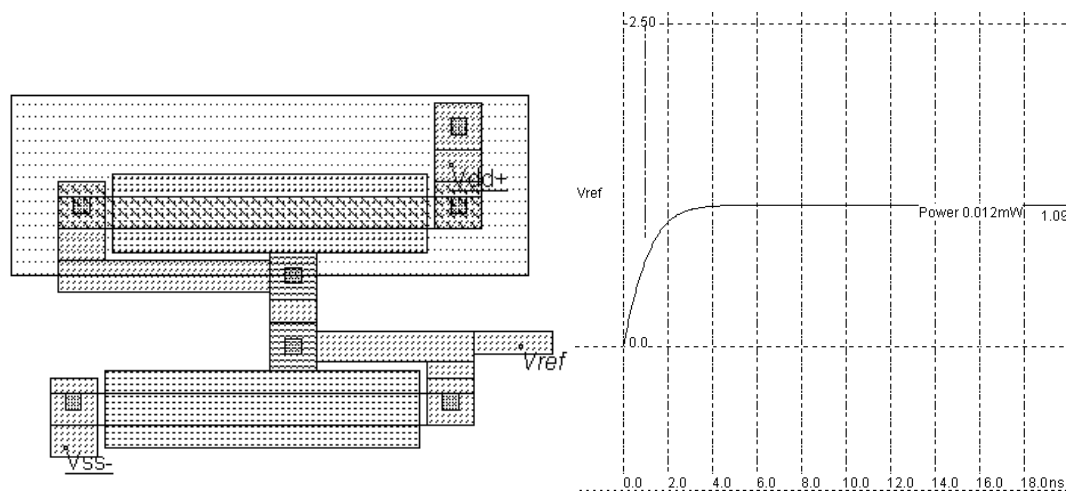


Figure 7-5 : Voltage reference of 1V (Vref.MSK)

In the layout of figure 7-5, the PMOS and NMOS have the same size. Due to lower PMOS mobility, the resulting Vref is not VDD/2 but 1V. You may change the temperature (Simulate -> Simulate Options) and see how the voltage reference is altered by temperature.

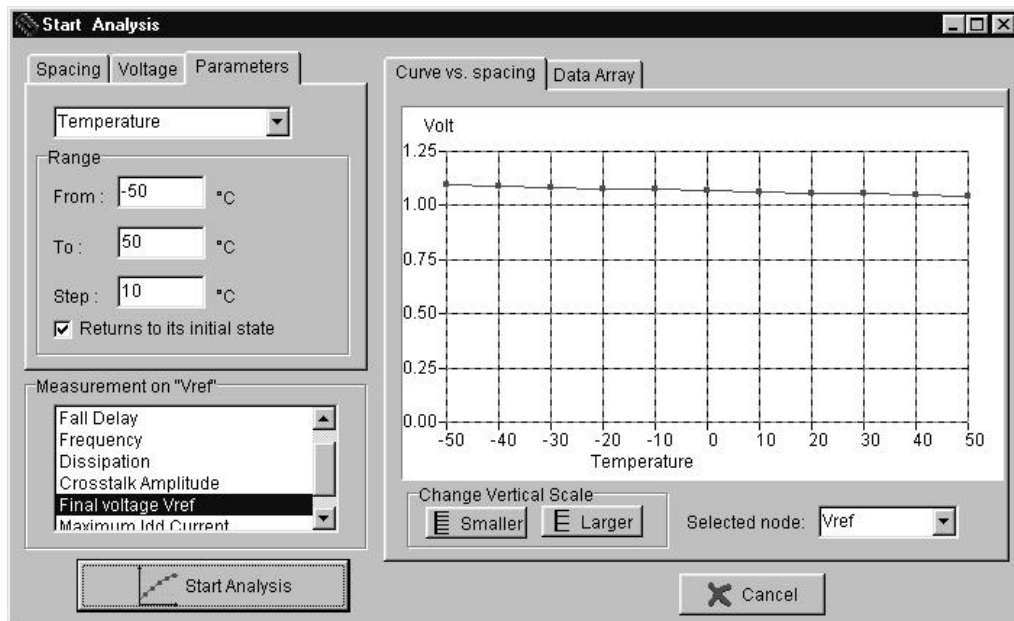


Figure 7-6 : Parametric analysis of the variation of Vref with temperature (Vref.MSK)

You may observe the variation of Vref for temperature varying from  $-50^{\circ}$  to  $+50^{\circ}\text{C}$  using a specific command called parametric analysis. Click "Analysis" -> "Parametric Analysis". Click on "Vref" with the mouse to indicate the node to perform the analysis. Then, click "Parameters" in the Analysis window, select temperature, and select "Final voltage" in the measurement list. Click "Start Analysis" (Fig. 7-6). In this design, Vref decrease from 1.1 to 1.04V when the temperature rises from  $-50^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ . Thus the thermal coefficient is negative, and roughly  $-6\text{mV}/^{\circ}\text{C}$ . Based on this principles, triple or quadruple voltage references can be designed. The limit is again the threshold voltage required for each stage.

## Current Mirror

The current mirror is one of the most useful basic blocs in analog design. In its most simple configuration, it consists in two MOS devices, as represented below. A current  $I_1$  flowing through the nMOS device Master is copied to the MOS device Slave. If the size of Master and Slave are identical, in most operating conditions, the currents are the same. The remarkable point is that the current is almost independent of the drain voltage of the slave  $V_2$ . If the ration W/L of the Slave is 10 times the ratio of the Master, the current on the right branch is 10 times the current on the left branch.

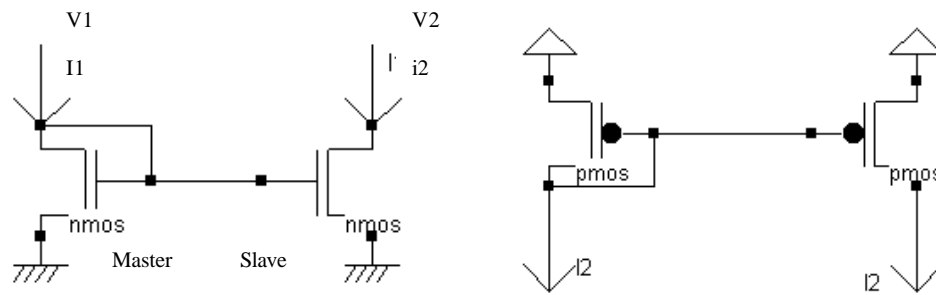


Figure 7-6: Current mirror principles in nMOS and pMOS versions

The illustration of the current mirror behavior is performed on the layout of figure 7.7. The circuit includes a voltage reference, using N1 and P1 as described above (See figure 7.5), a device N2 which has an identical size as N1, and a device N3 with  $L=0.5\mu\text{m}$ , leading to a ratio equal to 10  $W/L$  of N1. What we expect is a current  $I_2$  equal to  $I_1$  in most operating conditions and a current  $I_3=10 \times I_1$ .

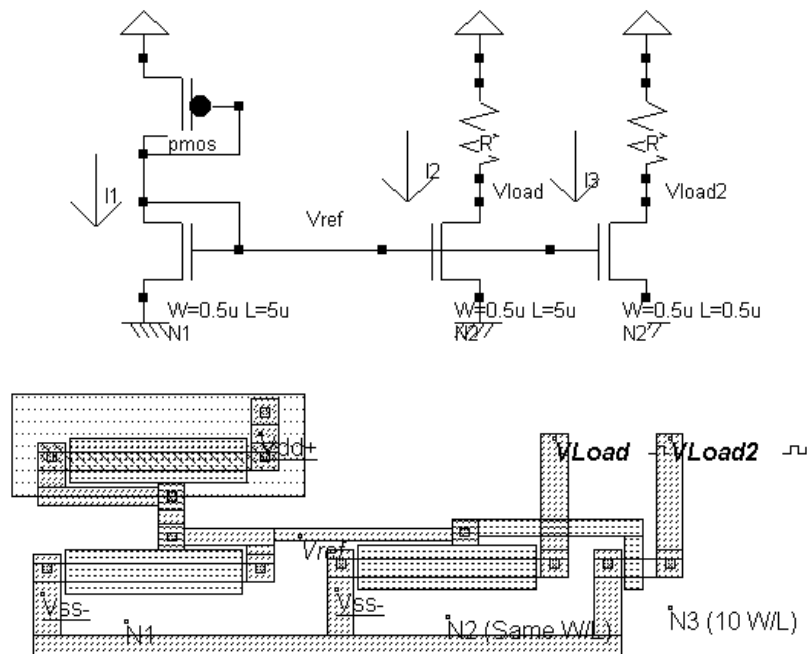


Figure 7-7: Illustration of the current mirror principles (Mirror.MSK)

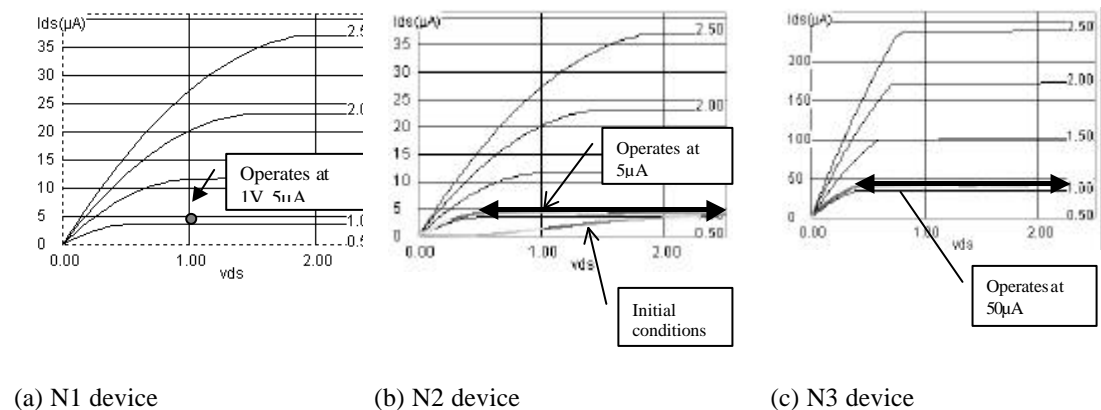
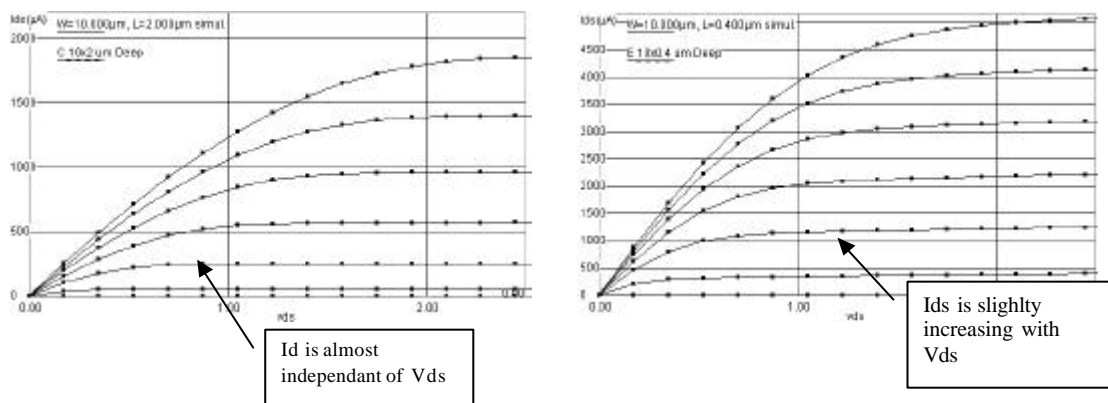


Figure 7-8: Simulation of the current mirror using direct layout simulation (Mirror.MSK)

You may observe each MOS characteristics by using the command **Simulate ® Simulate on Layout**. During the transient simulation, the functional point of the select MOS device appears in the characteristics, which provides a valuable aid to understand the current mirror behavior. In figure 7-8a, the device N1 operates at  $V_{ds}=1V$ , and a current of  $5\mu A$ . For most values of  $V_{load}$ , N2 also produces  $5\mu A$ , except when  $V_{load}$  is lower than  $0.5V$  (Figure 7-8b). Consequently, the current  $I_{ref}$  is copied to  $I_2$ . At the same time, N3 produces  $50\mu A$ , almost independently of the value of  $V_{load2}$ . This demonstrates that  $I_3$  is  $10 \times I_1$ .

### IMPROVING THE CURRENT MIRROR PERFORMANCES



(a)  $L=2\mu m$

(b)  $L=0.35\mu m$

Figure 7-9: Long channel MOS are preferred for high performance current mirrors (Ma10x2.MES, Ma10x0,4.MES)

As the basic principles of the current copy is the assumption that  $I_d$  is independent of  $V_{ds}$ , the long channel MOS (Fig 7-9a) is a better candidate than the short channel MOS (Fig 7-9b). Although the short channel MOS works better in standard logic, the long channel MOS is preferred for a high precision copying of currents.

### IMPROVING THE MOS MATCHING

A set of design techniques can improve the current mirror behavior, as illustrated in figure 7-10.

- All MOS devices should have the same orientation. During fabrication, the chemical process has proven to be slightly different depending on the orientation, resulting in variations of effective channel length. This mismatch alters the current duplication.
- Long channel MOS devices are preferred. In such devices, the channel length modulation is small, and consequently  $I_{ds}$  is almost independent of  $V_{ds}$ .

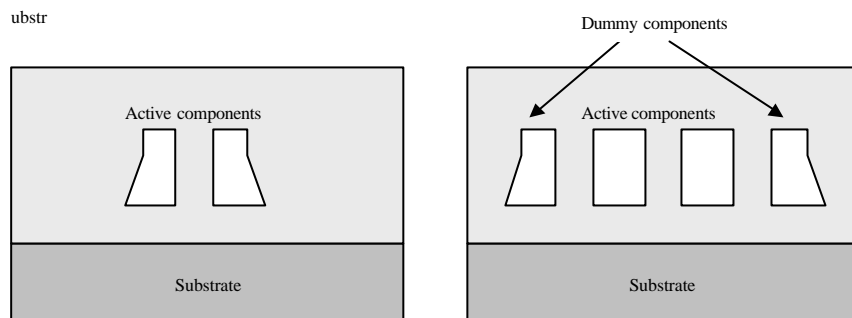


Figure 7-xxx: 2D aspect of the circuit without and with dummy components

- Dummy gates should be added at both sides of the current mirror. Although some silicon area is lost, due to the addition of inactive components, the patterning of active gates leads to very regular structures, ensuring a high quality matching (See figure 7-xxx).
- MOS devices should be in parallel. If possible, portions of the two MOS devices should be interleaved, to reduce the impact of an always-possible gradient of resistance, or capacitance with the location within the substrate.

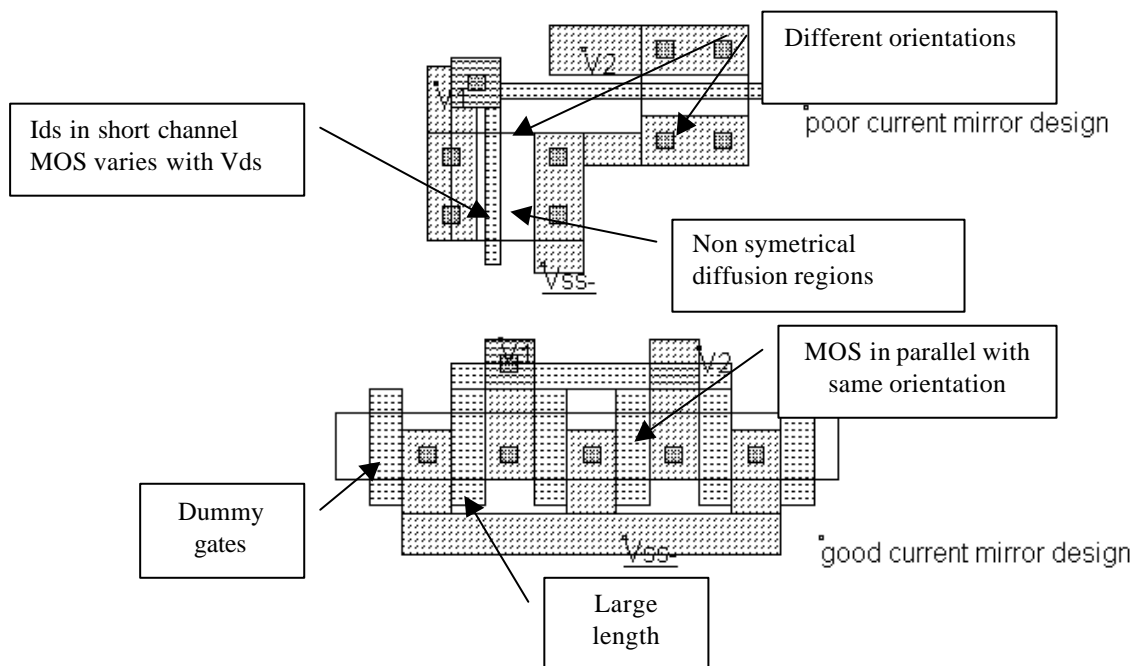


Figure 7-10: Design of high performance current mirrors (MirrorMatch.MSK)

## Single Stage Amplifier

The single-stage amplifier is described in figure 7-11a. It consists of a MOS device (we choose here a n-channel MOS) and a load resistance. The resistance can be made from polysilicon or diffusion. As the gain of this amplifier is proportional to the load resistance, a MOS device with gate and drain connected, as shown in figure 7-11b could replace the resistance. This is called an active resistance. Using a small silicon area, high resistance can be obtained, meaning high amplifier gains.

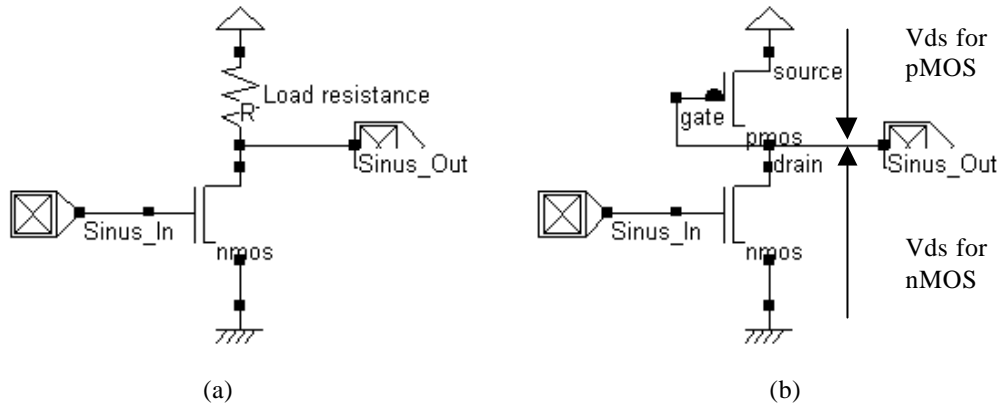


Figure 7-11: Single stage amplifier with passive resistance (a) and active resistance (b).

We define the transconductance  $g_m$  as the derivative of  $i_{DS}$  versus  $v_{DS}$ . Thus  $g_m$  is the invert of the channel resistance. Using the very simple approximation of the MOS current (2) in saturation (See chapter 2 for details on the MOS model 1), a formulation of  $g_m$  in saturation is obtained (3). Now, we add to  $V_{DS}$  a small sinusoidal input  $v_{ds}$ . Consequently, a small variation of current  $i_s$  is added to the static current  $I_{DS}$ . For small variations of  $v_{ds}$ , the link between the variation of current  $i_s$  and the variation of voltage  $v_{ds}$  can be approximated by (4). Thus, the gain of the amplifier can be expressed by (5).

$$g_{mos} = \left[ \frac{\partial I_{DS}}{\partial V_{GS}} \right] \quad (1)$$

$$I_{DS} = \frac{K_p}{2} \frac{W}{L} (V_{GS} - V_T)^2 \quad (2)$$

$$g_m = K_p \frac{W}{L} (V_{GS} - V_T) \quad (3)$$

$$i_{ds} = g_m v_{gs} \quad (4)$$

$$Gain = \frac{Sinus\_Out}{Sinus\_In} = \frac{-i_{ds} \frac{1}{g_{pmos}}}{i_{ds} \frac{1}{g_{nmos}}} = -\frac{g_{nmos}}{g_{pmos}} \quad (5)$$



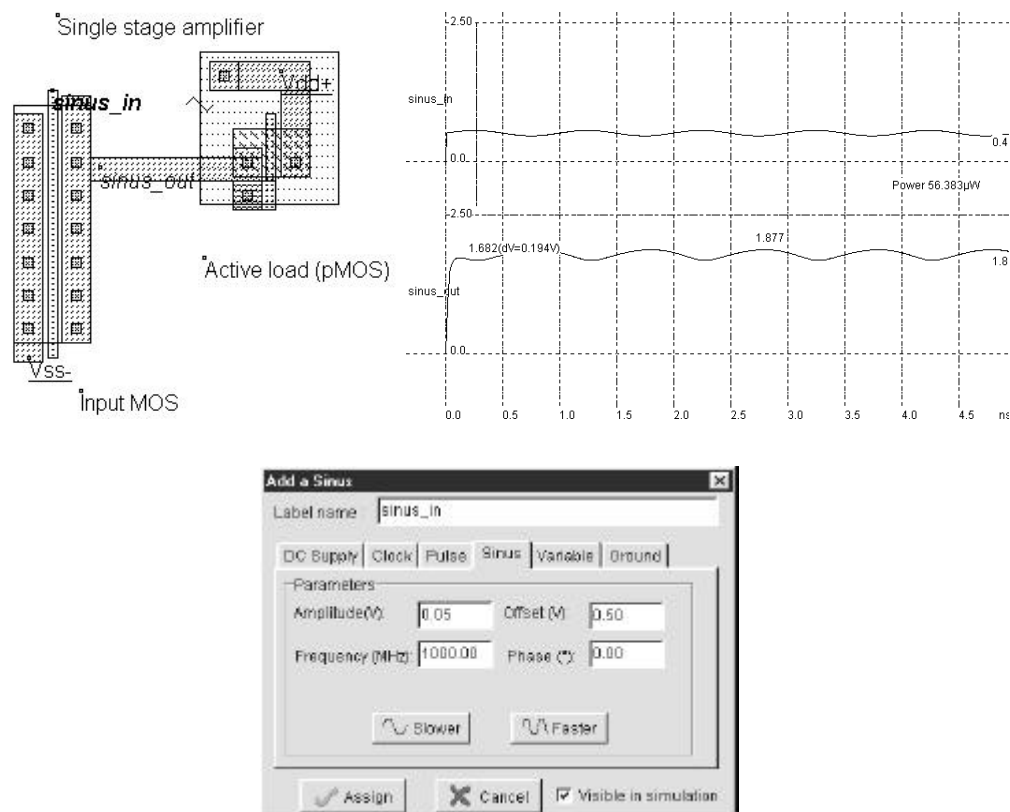


Figure 7-12: Single Stage amplifier layout and simulation (AmpliSingle.MSK)

The time-domain simulation of the amplifier with a 50mV 1GHz sinusoidal input (0.3V offset) exhibits very poor performances: the measured gain is less than 2. In the simulation window, click “Voltage vs voltage” and “More”, to compute the static response of the amplifier (Figure 7-13). The range of voltage input that exhibits a constant gain appears clearly. For  $V_{DS}$  higher than 0.6V and lower than 0.8V, the output gain is around 5. Therefore, an optimum offset value is 0.7V. Change the parameter "Offset" of the input sinusoidal wave to place the input voltage in the correct polarization.

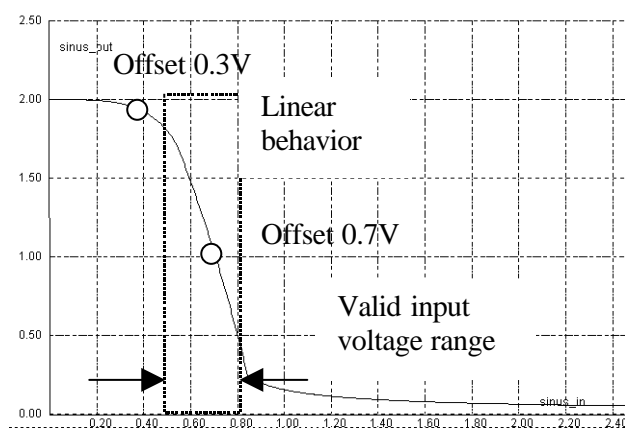


Figure 7-13: Single Stage amplifier static response

We change the sinusoidal input offset and start again the simulation. A gain of 5 is observed as predicted from the static simulation when the offset is 0.8V (input 100mV peak to peak, output 482mV peak to peak).

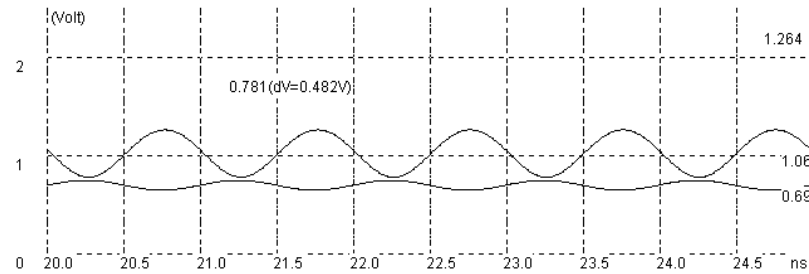


Figure 7-14: Single Stage amplifier with high gain

To further increase the gain, the ratio between the active load resistance and the n-channel MOS resistance should be increased. In the layout file AmpliSingle2.MSK, two single amplifiers are designed, one with a pMOS with low resistance (left sinus1), the other with high resistance (right sinus2). The gain for sinus2 is improved, as observed in figure 7-xxx, with sharper characteristics, but the input voltage range that features amplification becomes narrow.

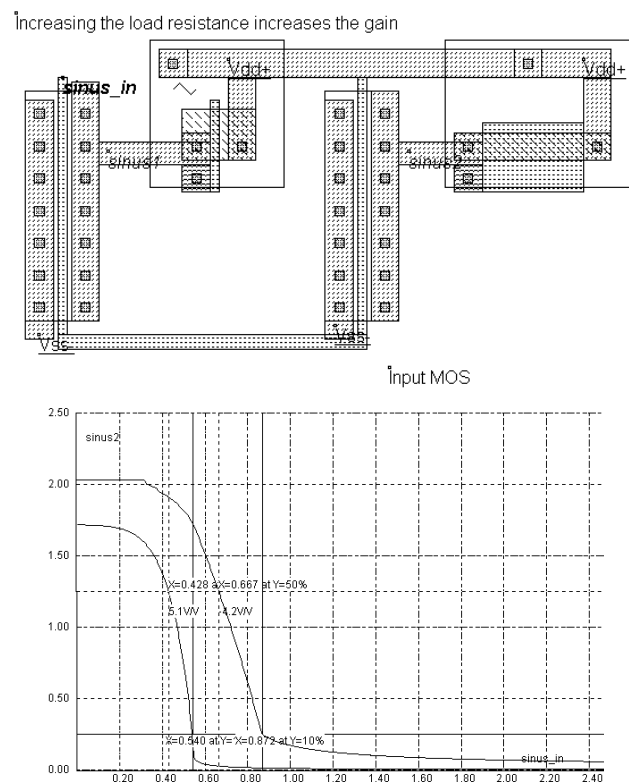


Figure 7-xxx: The active load sizing acts on the gain, but reduces the input voltage range for amplification (AmpliSingle2.MSK)

## The Inverter as Amplifier

Could the logic CMOS inverter act as an amplifier? In principles, yes, as the static characteristics of the CMOS amplifier (See figure below) is very much like the static response of the basic amplifier described earlier. The main problem is the very high gain of the amplifier. When trying to compute the slope, we find 180. To operate in the amplifier zone, we should inject a signal around 1.20V, otherwise there is no chance to take advantage of the very high amplification.

Furthermore, as the process parameters are not well controlled, the commutation point of the inverter may fluctuate in a significant range, depending on the location of the die on the wafer, or even on the die itself. As a consequence, very high gain structures are not adequate. Usually, amplifiers with gain around 10 (that is 20dB) are used, for example in the low noise input amplifier of the GSM.

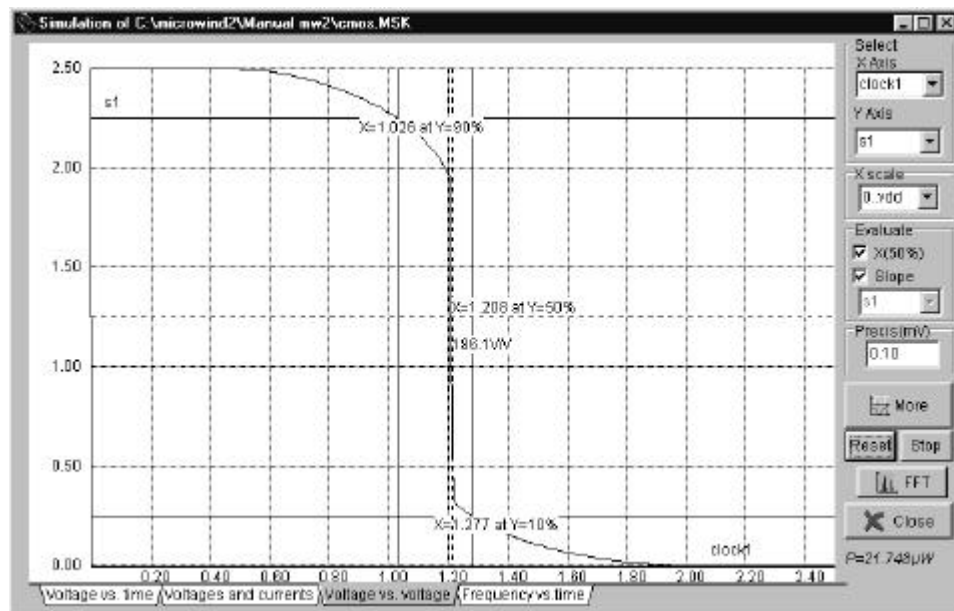


Figure 7-xxx: CMOS inverter as a single stage amplifier

## Simple Differential Amplifier

The goal of the differential amplifier is to compare two analog signals, and to amplify their difference. The differential amplifier formulation is reported below. Usually, the gain  $K$  is high, ranging from 10 to 1000. The consequence is that the differential amplifier output saturates very rapidly, because of the supply voltage limits.

$$V_{out} = K(V_p - V_m)$$

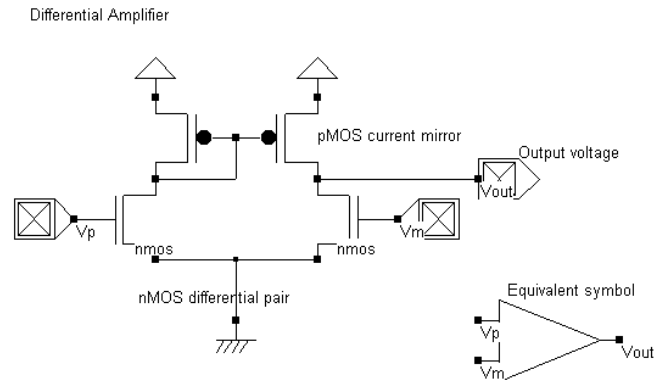


Figure 7-15: Schematic diagram of the differential amplifier

The differential amplifier layout is reported in figure 7-16. The differential pair is built from n-channel MOS devices. Their size must be identical, and drawn with the same orientation, to minimize the offset generated by transistor mismatch. In the simulation, it can be seen that a small voltage difference between  $V_+$  and  $V_-$  induces the saturation of the output either near  $V_{SS}$  and  $V_{DD}$ .

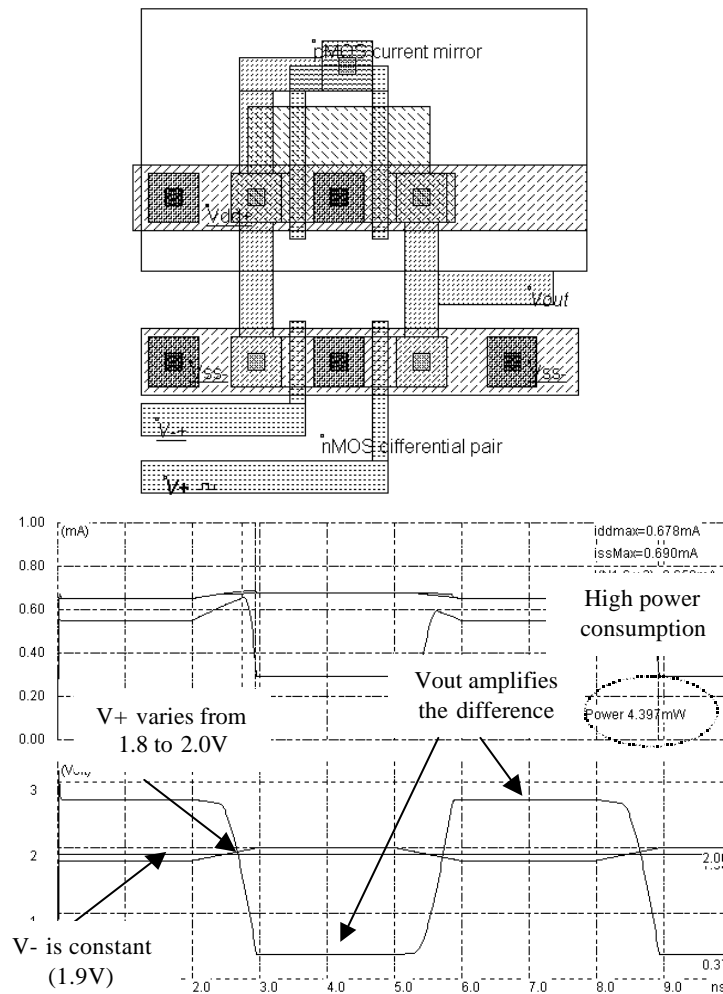


Figure 7-16: Layout and transient simulation of the differential amplifier (AmpliDiff.MSK)

## MEASURE THE GAIN

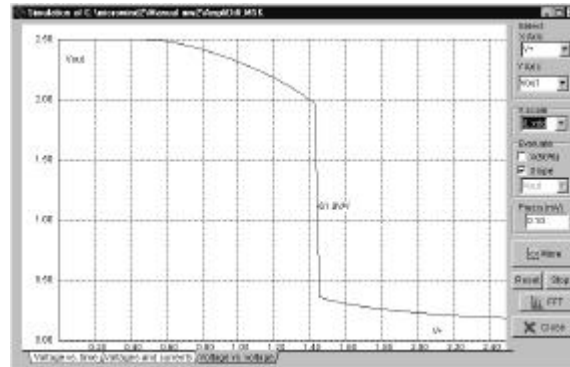


Figure 7-17: Computing the gain of the differential amplifier (AmpliDiff.MSK)

1. Click « Voltage vs. Voltage » to select static characteristics mode.
2. Select « Slope » in the « Evaluate » menu.
3. Click « More » to compute the static characteristics of the differential amplifier. A gain higher than 60 is added on the simulations.

## MEASURE THE INPUT RANGE

The best way to measure the input range is to connect the differential amplifier as a follower, that is  $V_{out}$  connect to  $V_-$ . In this case, a slow ramp is applied on the input  $V_+$  and the result is observed on the output. The valid input range  $[0.5, 1.9V]$  is the value of  $V_+$  for which the output copies the same voltage in a reasonable time.

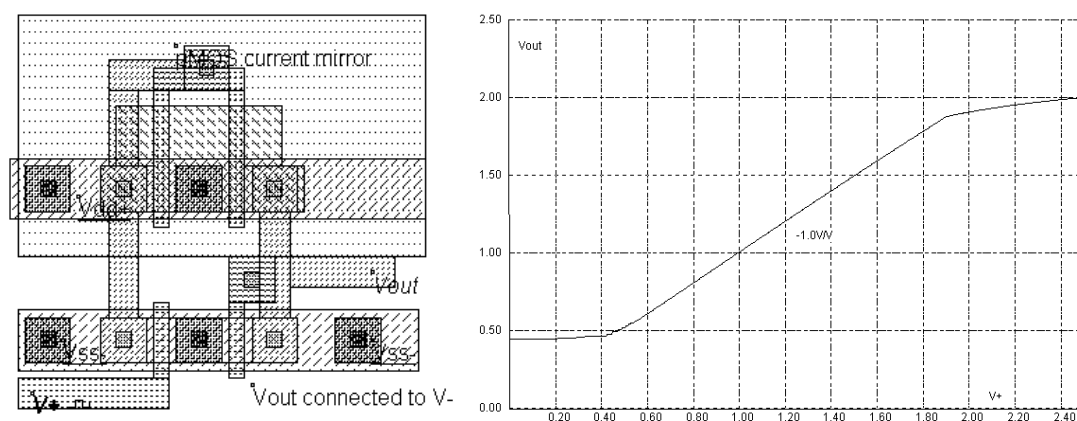


Figure 7-18: Computing the input range in follower mode (AmpliDiff2.MSK)

## Wide-Range Amplifier

The wide-range amplifier is built using a voltage comparator and a power output stage. Its schematic diagram is reported in Fig. 7-19. The difference between  $V_+$  and  $V_-$  is amplified and it produces a result, codified :  $V_{out}$ . The gain near 2.5V is more than 1,000. Use the **Voltage vs. Voltage** simulator mode to get the transfer characteristics  $V_{out}/V_+$ . The input range is around 0.5V to 4.0V.

You can easily build a follower by designing an extra connection from  $V_{out}$  to  $V_-$ . This layout is shown in Figure 66. The output stage is not strong enough to be able to drive large loads such as output pads.

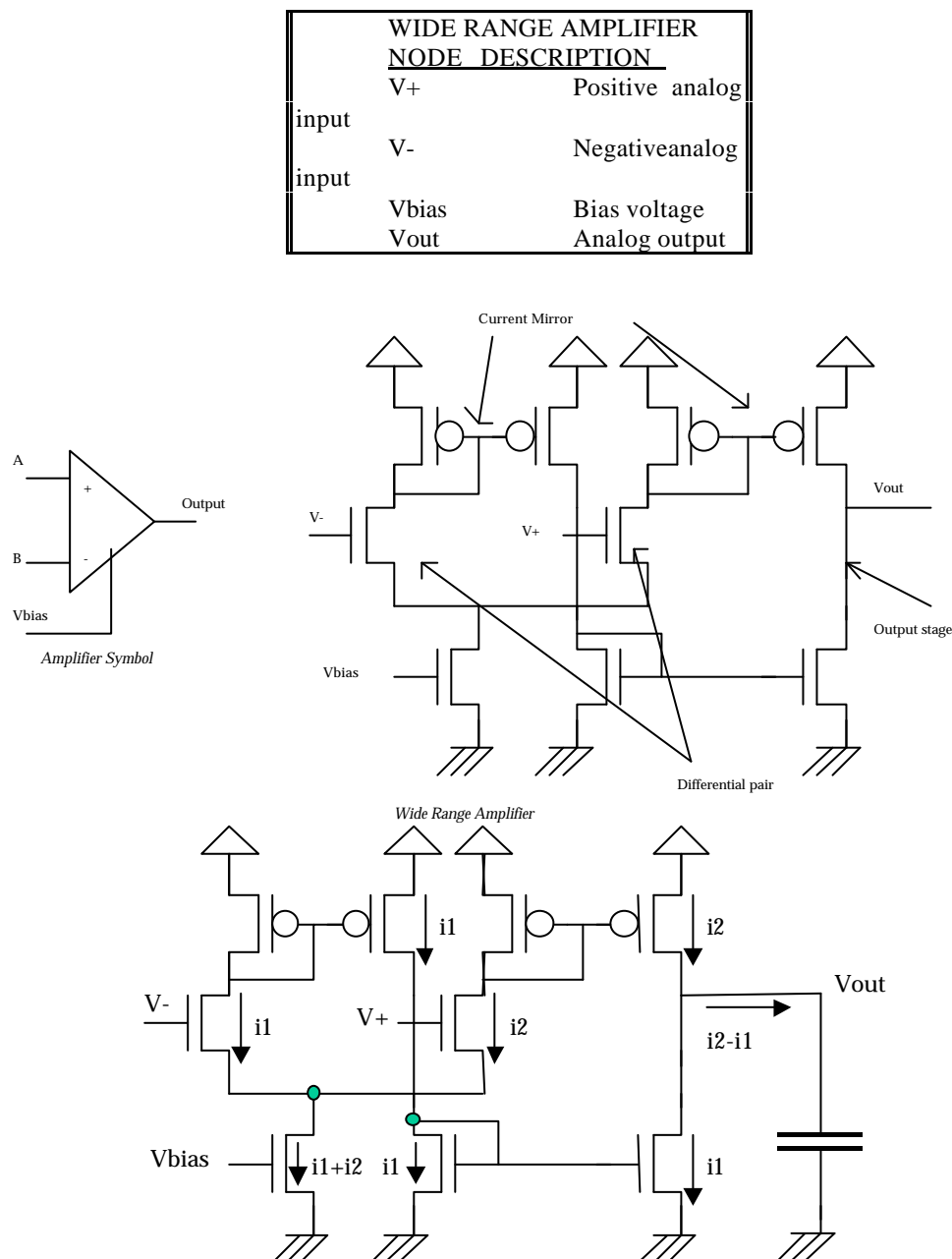


Fig. 7-19. Node description and schematic diagram of the analog amplifier (AMPLI2.MSK).

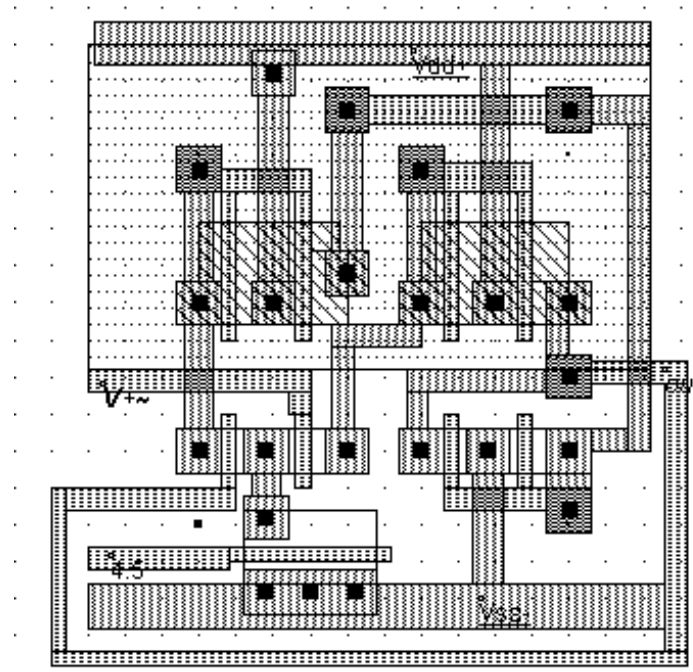


Fig. 7-20 Design of the analog amplifier (AMPLI2.MSK).

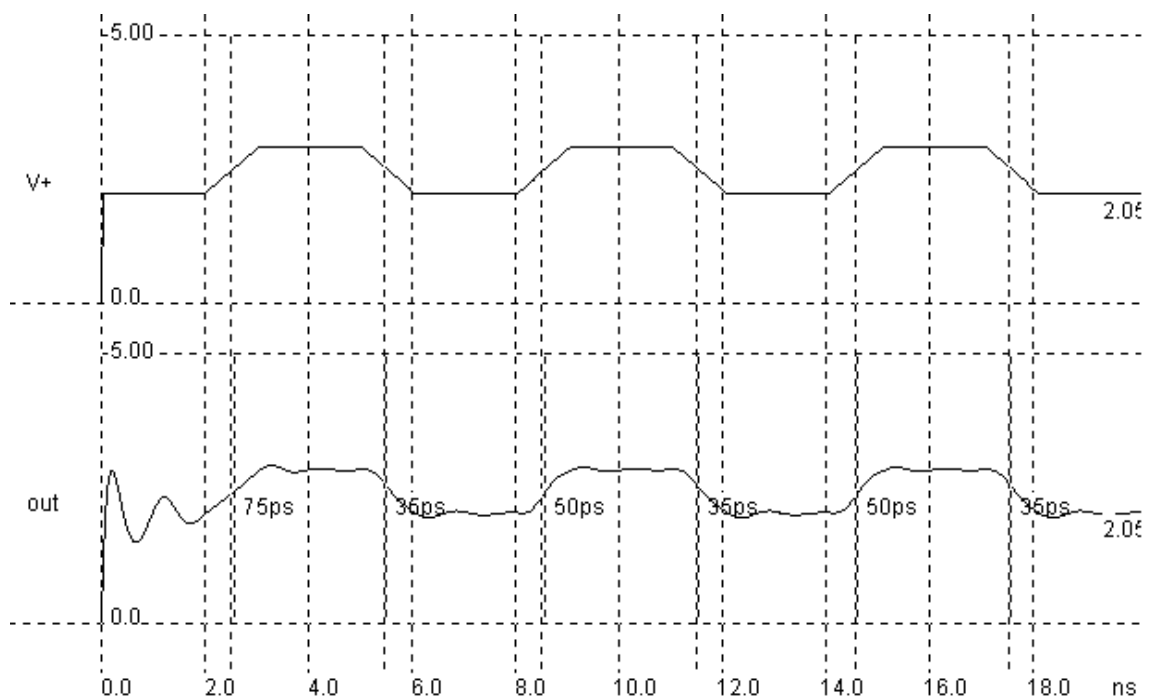


Fig. 7-21. Transient simulation of the analog amplifier (AMPLI2.MSK) connected as a follower

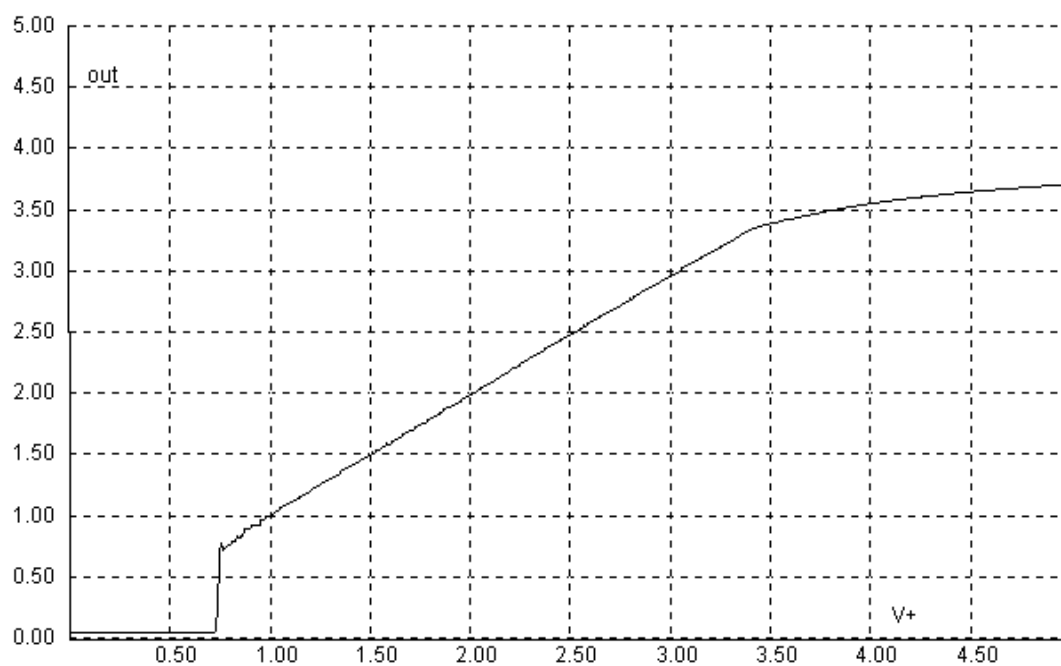


Fig. 7-22. DC Simulation of the analog amplifier (AMPLI2.MSK) in follower mode, using **voltage vs. Voltage** mode.



## On-chip Voltage Regulator

In deep sub-micron technology, the use of very thin gate oxide implies a low supply voltage. This supply decrease is mainly due to the increased risk of damaging the oxide that separates the gate from the drain and source regions, when high voltage differences are present. In contrast, the input/output interface of the integrated circuit must meet standard requirements in terms of voltage, basically 5V or 3.3 V supply. This means that a specific circuit must be designed to generate a low voltage source internally from an external high voltage supply.

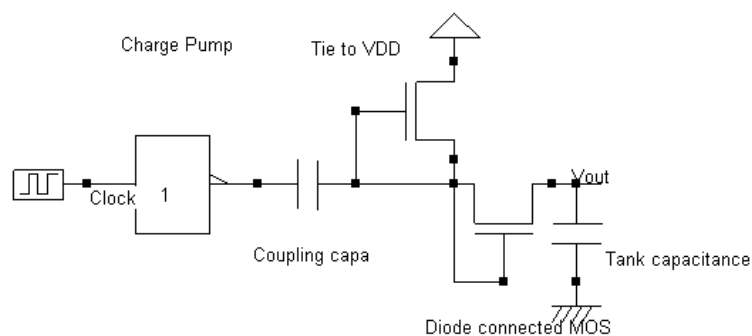
Figure 7-23 illustrates the principles of an on-chip voltage regulator. The circuit is simply an operational amplifier which compares a voltage reference to the internal supply voltage.

<To be added>

*Figure 7-23 : Schematic diagram of an on-chip voltage regulator*

## Charge Pump

The charge pump is an analog circuit that can generate a voltage supply higher than its own supply voltage. For example, with a supply 2.5V, the circuit of figure 7-xxx can generate 3V. The principles of the charge pump is to charge a capacitance C through an inverter, creating crosstalk overshoots and undershoots. We use a diode-connected MOS to keep half of the signal, the positive one in our case. Slowly, the output rises to voltages higher than the supply. After several clock cycles,  $V_{out}$  rises to 3.0V. Increasing the coupling capacitance increases the charge pump efficiency.



*Figure 7-xxx : Schematic diagram of the charge pump*

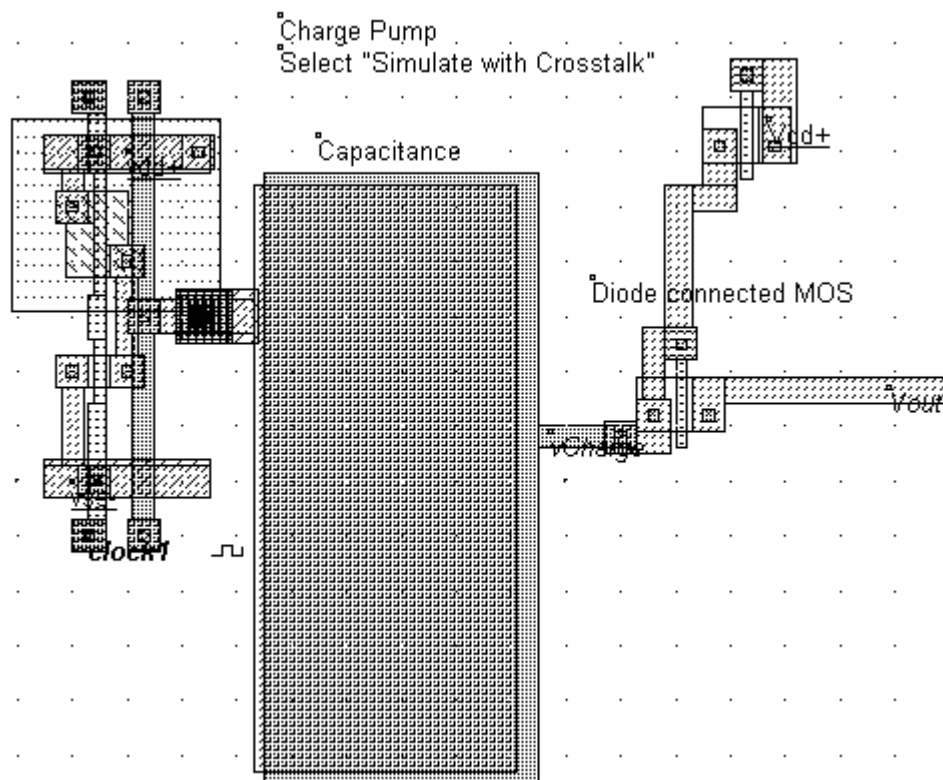


Figure 7-xxx : Layout of the charge pump

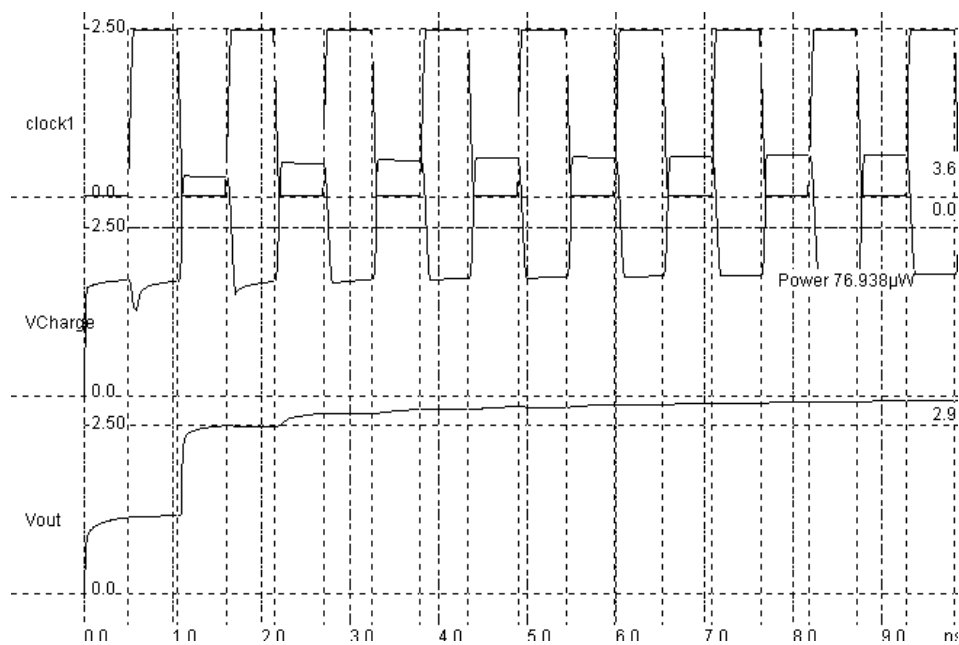


Figure 7-xxx : Simulation of the charge pump

## Phase-Lock Loop

The phase-lock-loop is commonly used in microprocessors to generate a clock at high frequency ( $F_{out}=512\text{MHz}$  for example) from an external clock at low frequency ( $F_{ref} = 16\text{MHz}$  for example). The PLL uses a counter, which divides a high input frequency  $F_{out}$  into a low output frequency (divide by 32 in the example), which is tuned to fit exactly with the reference frequency  $F_{ref}$ . The basic schematic diagram of this function is reported below.

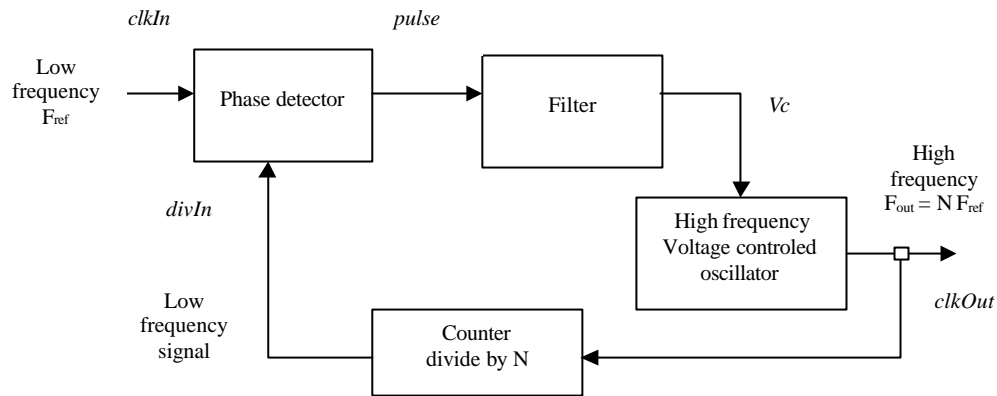


Fig. 7-24. Principles of phase lock loops

### PHASE DETECTOR

The most simple phase detector is the XOR gate. The XOR gate output produces a regular square oscillation when the input  $clkIn$  and the signal  $divIn$  have one quarter of period shift (or  $90^\circ$  or  $\pi/2$ ). In figure 7-xxx, two clocks with slightly different periods are used in Dsch2 to illustrate the phase detection.

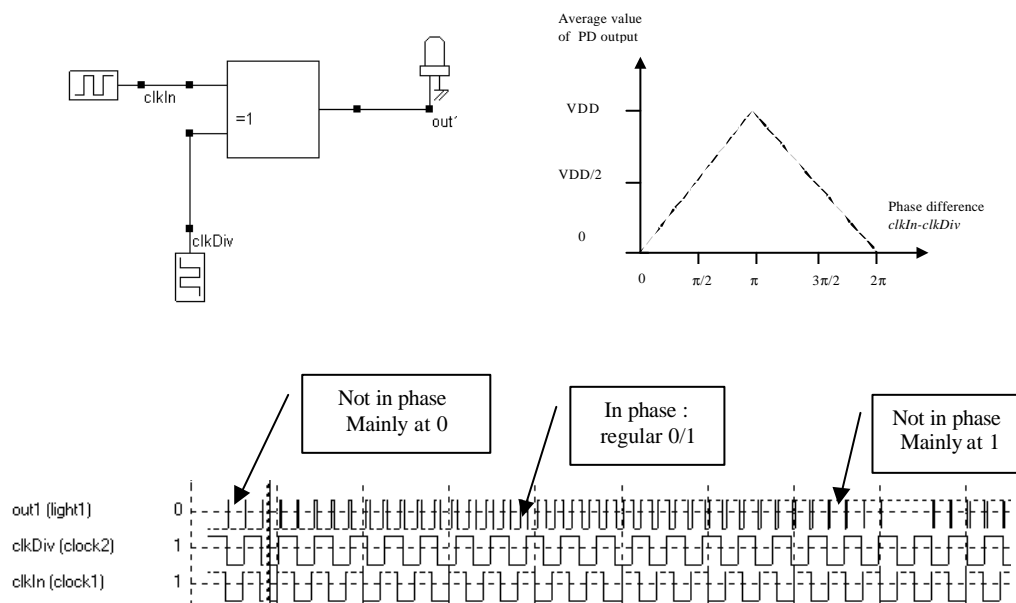


Fig. 7-25. Principles of phase lock loops

At initialization, (Figure 7-26) the average value of the XOR output is close from 0. When the phase between clkDiv and clkIn is around  $\pi/2$ , the average value of the XOR output is  $V_{DD}/2$ . Then it increases up to  $V_{DD}$ .

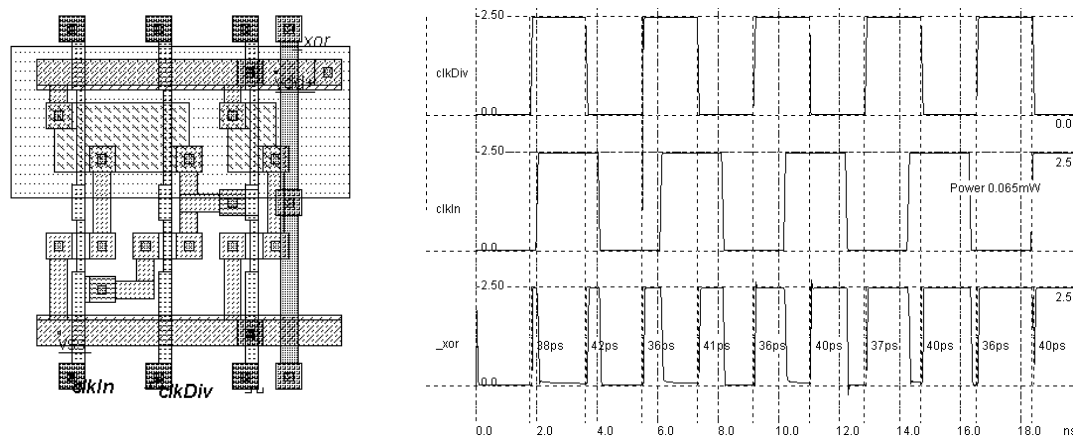


Fig. 7-26. Using the XOR gate to illustrate the phase detection at logic and layout level

## FILTER

The filter is simply a capacitance. The highest value for capacitance is the gate capacitance, thanks to a very thin gate oxide that produces a high density capacitance. Also worth of interest are the N+/P\_substrate and P+/N\_well junctions. Figure 7-27 shows an XOR gate with output charged with a large gate capacitance (around 200fF).

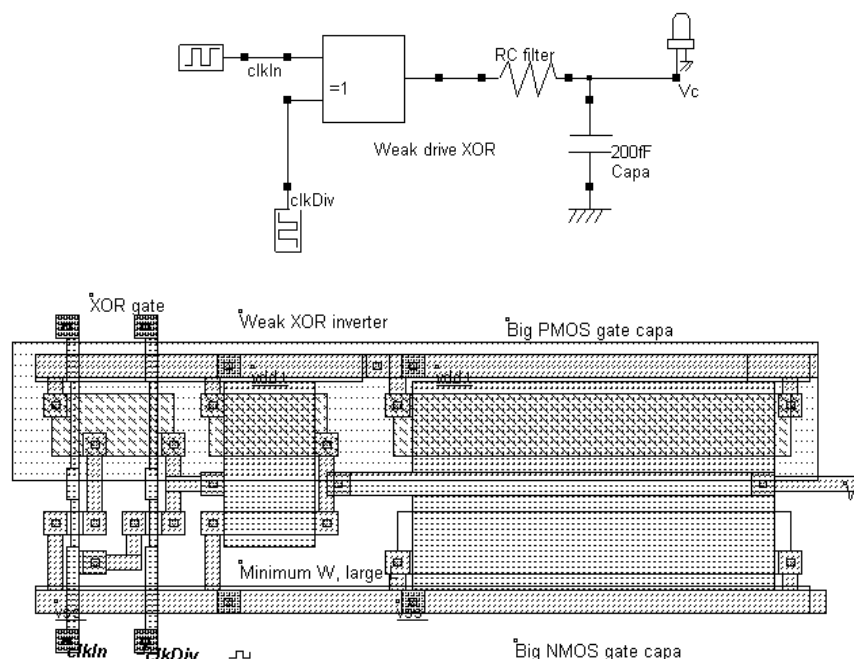


Fig. 7-27. Large load capacitance and weak XOR output stage to act as a filter (phaseDetect.MSK)

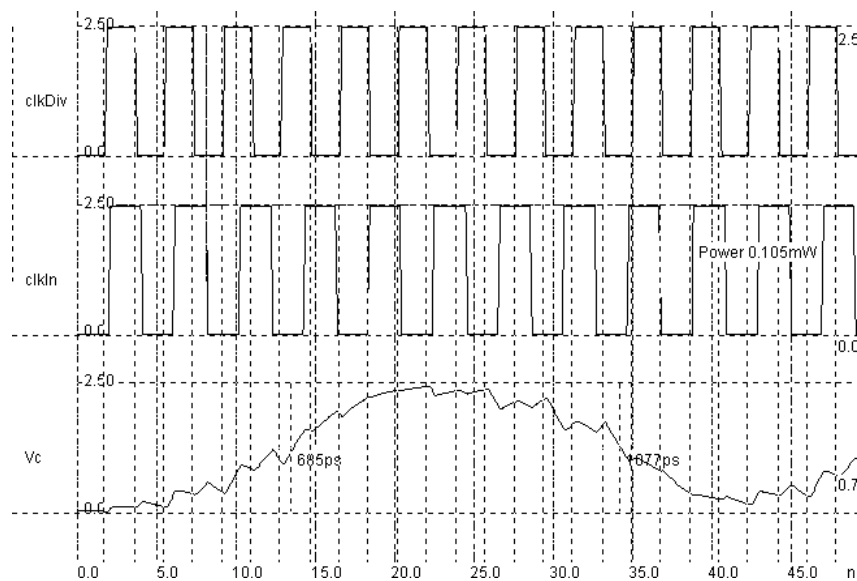


Fig. 7-28. Response of the phase detector to slightly different input clocks (phaseDetect.MSK)

In the figure above, the filtered version of the XOR gate output is shown. Although some further filtering are required, it can be seen that  $V_c$  is around  $V_{DD}/2$  when the phase difference is  $\pi/2$  or  $-\pi/2$ .

#### VOLTAGE CONTROLLED OSCILLATOR

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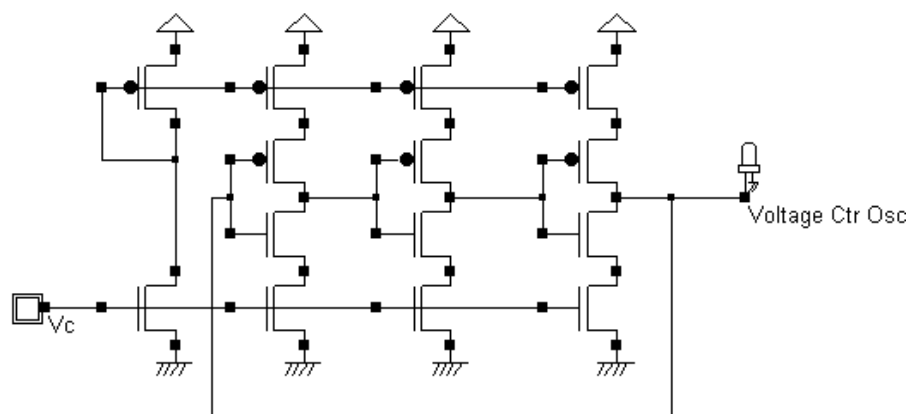


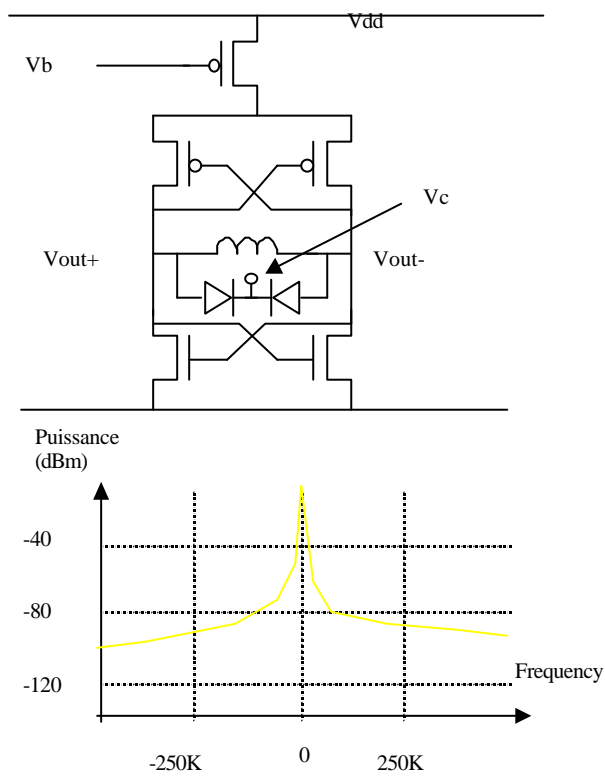
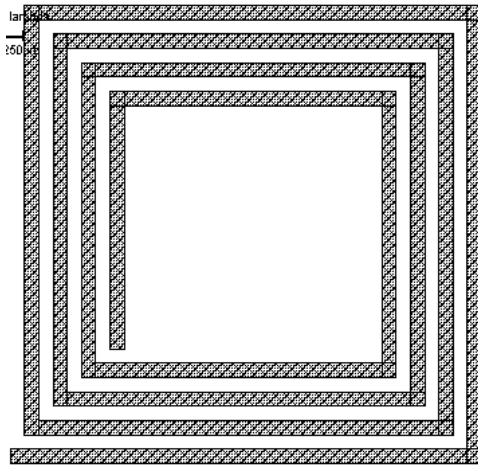
Fig. 7-29. Schematic diagram of a voltage controlled oscillator

#### COMPLETE PHASE LOCK LOOP

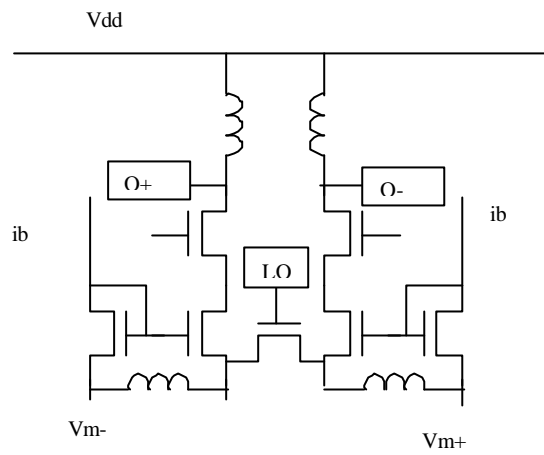
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## Oscillator for GSM



## Upconverter for GSM



## Down-converter for GSM

