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# 10

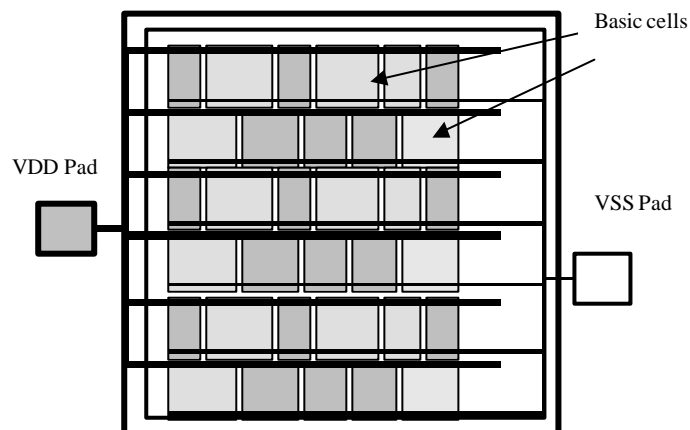
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## Input/Output Interfacing

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### VDD/VSS Floor-planning

The supply network of a typical integrated circuit is shown in figure 10-1. Bars of metal wires cross the circuit to supply the active parts of the circuit. The metal wires are designed very large to enable strong currents to flow within the supply interconnects.



*Fig. 10-1. Supply of an integrated circuit*

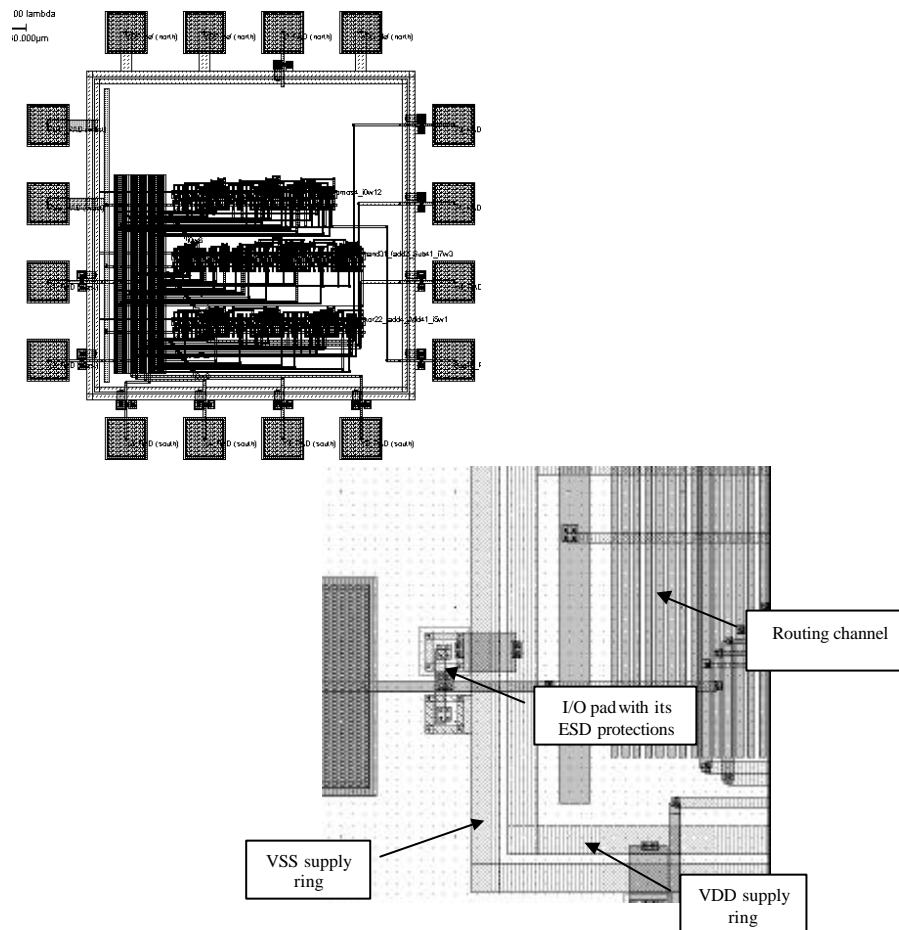


Fig. 10-2: Supply network in a real case circuit

## High Voltage MOS

For interfacing with input/output, specific high voltage MOS are introduced. These MOS devices are called high voltage MOS. They use a thick gate oxide to handle the high voltage of the I/Os. An example of high voltage MOS device is reported below.

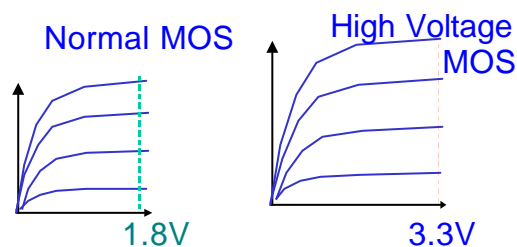


Fig. 10-3: The High voltage MOS device is used in 3.3V I/Os

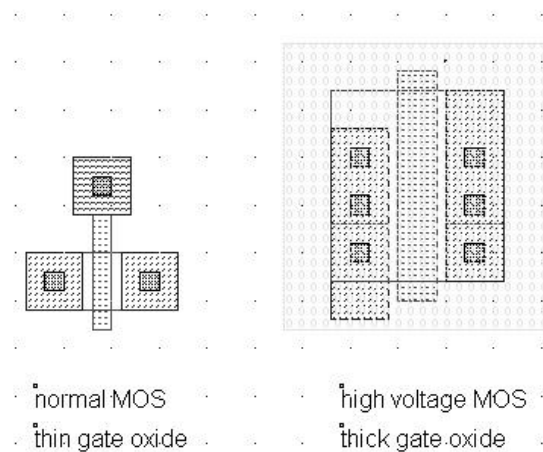


Fig. 10-3: High voltage MOS device

In the layout of figure 10-4, the high voltage MOS uses a gate width which is slightly larger than the one of the regular MOS. As the high voltage MOS device is generally used in I/O structures, the MOS width is usually large, even sometimes very large (100-500 $\mu$ m).

## Level Shifter

In deep submicron technology, the core supply is low, as the gate oxide is extremely thin. For example in CMOS 0.25 $\mu$ m the internal supply is 2.5V. Anyhow, for compatibility reasons, the interfacing with the external components has been maintained to 3.3V. Thus a voltage translator is required to convert the internal logic data working from 0 to 2.5V into a logic data working from 0V to 3.3V.

Figure 10-xxx gives the schematic diagram of such a circuit. The layout is also shown, together with the time domain simulation.

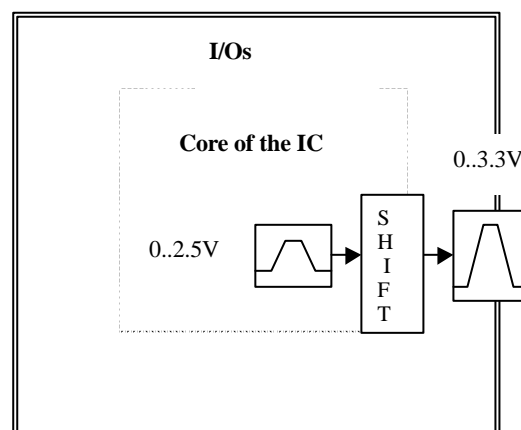


Fig. 10-xxx: Level shifter

Fig. 10-xxx: Level shifter structure & layout

*Fig. 10-xxx: Simulation of the level shifter*

## I/O Pad

We give here some details about input-output pad structure. The basic bonding pad size is  $100 \times 100 \mu\text{m}$ . The pad consists of a sandwich of **metal** layers. For advanced technologies, all metal layers are stacked on the top of each other. The passivation oxide has been removed from over the pad, so that a gold connection can be fixed upon it. The input-output pad contains one input stage with a polysilicon resistor and two protection diodes. The output stage contains a chain of inverters. The last stage is a 3-state inverter so that the buffer can be turned off.

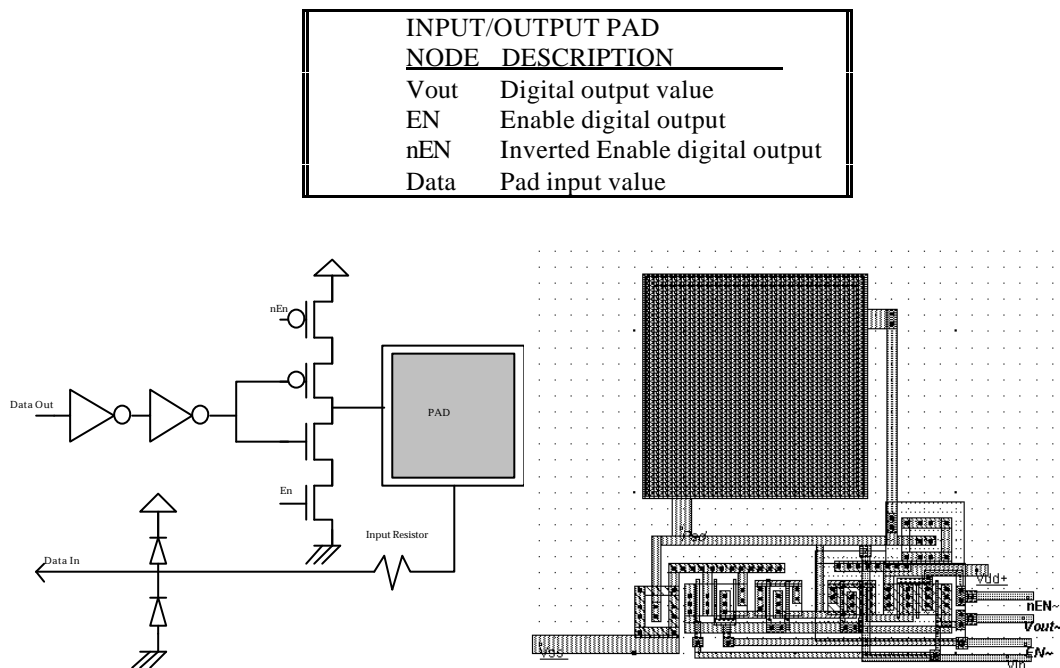


Fig. 10-3. Design of an input-output pad (PAD.MSK)

## Input noise filtering: the trigger

The schematic diagram of the trigger is proposed in figure 10-xxx.

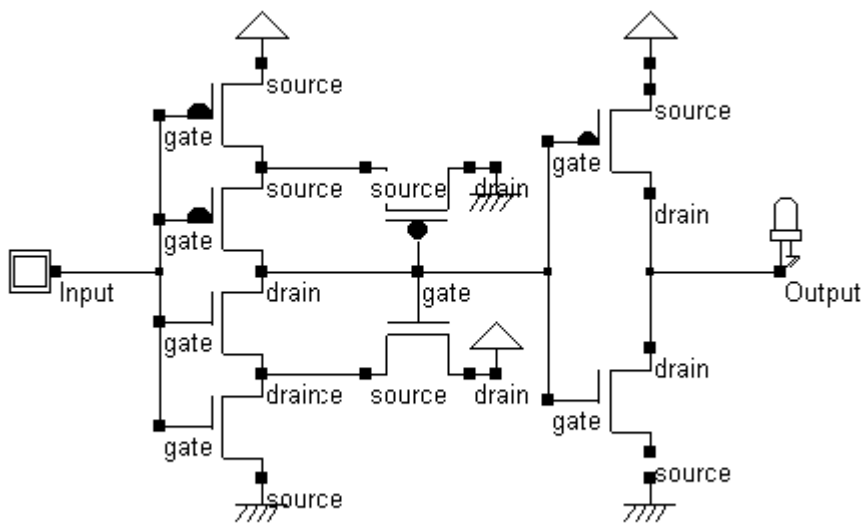


Fig. 10-xxx. Schematic diagram of the trigger (TRIGGER.SCH)

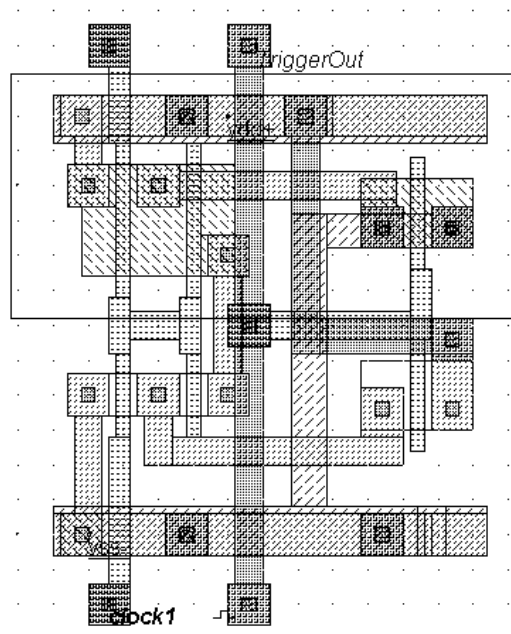


Fig. 10-xxx. Layout of the trigger (TRIGGER.SCH)

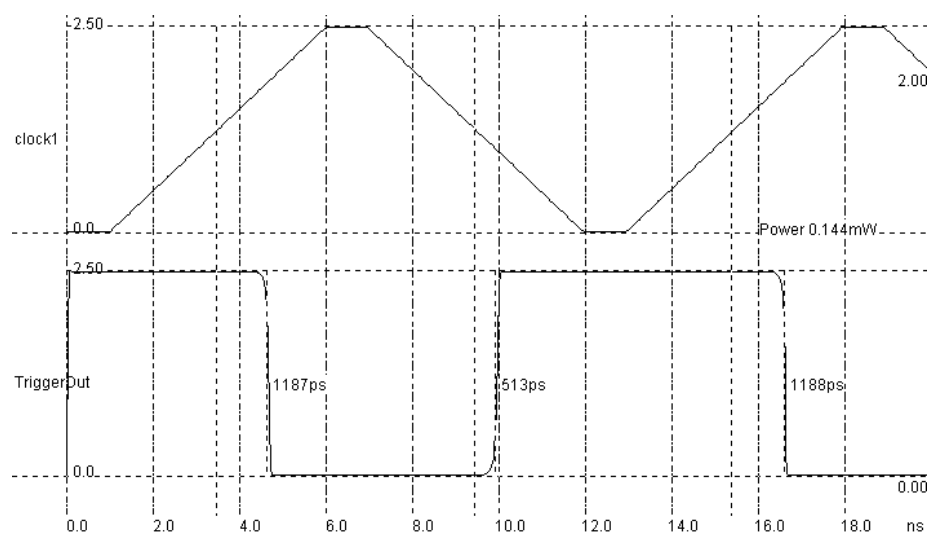


Fig. 10-xxx. Analog simulation of the trigger (TRIGGER.SCH)

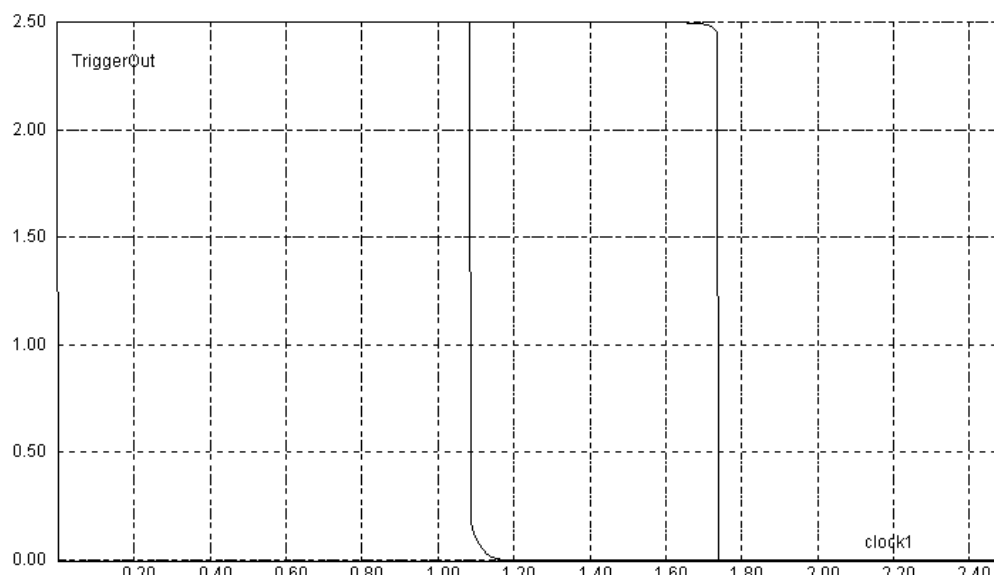


Fig. 10-xxx. Analog simulation of the trigger (TRIGGER.SCH)

Noise analysis: <Add noise>

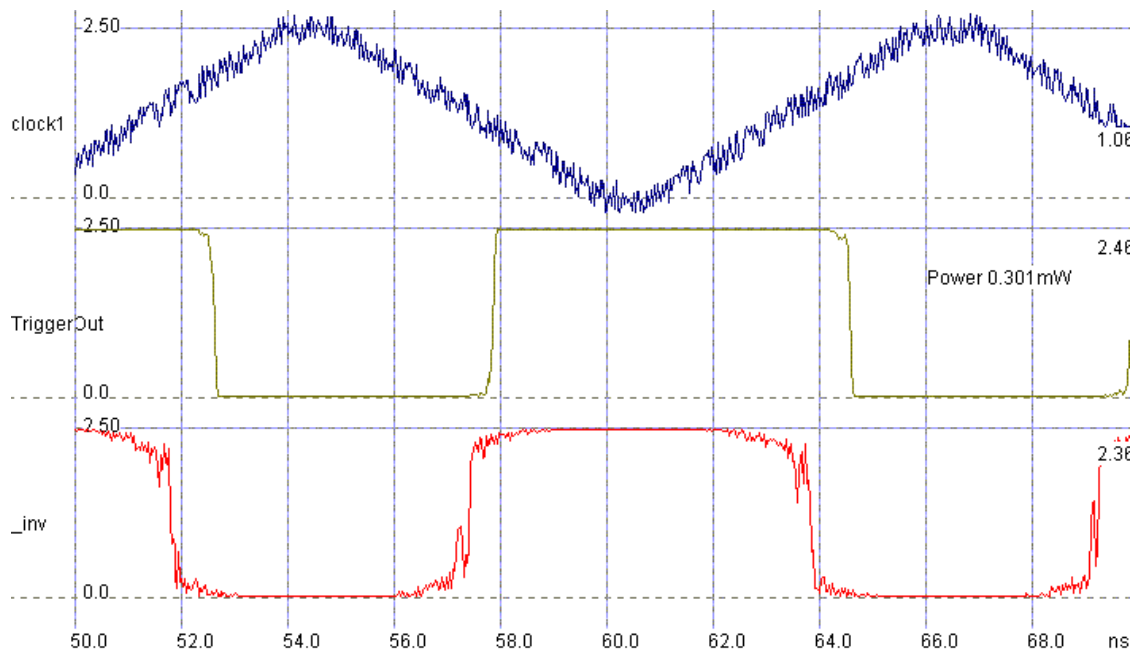


Fig. 10-xxx. Utility of the trigger to filter noise (TRIGGERCOMPINV.SCH)

## Pad Ring



Click on the chip library icon and click on **Pads**. The window reported in Fig. 10-4 appears. Enable the “pad ring” option. A pad ring with 3 pads in X and 3 pads in Y is generated by a click on **Generate Pad**. In that case, a set of pads is added to your circuit. The VSS pad is situated at the bottom, and the VDD pad at the top with the associated power rings.

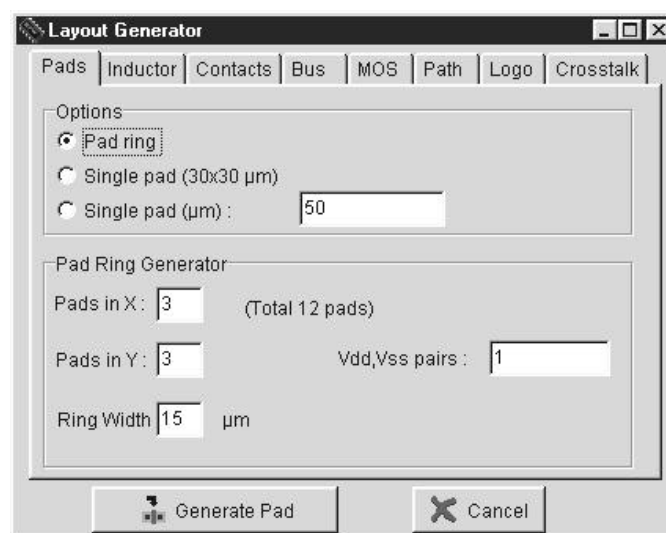
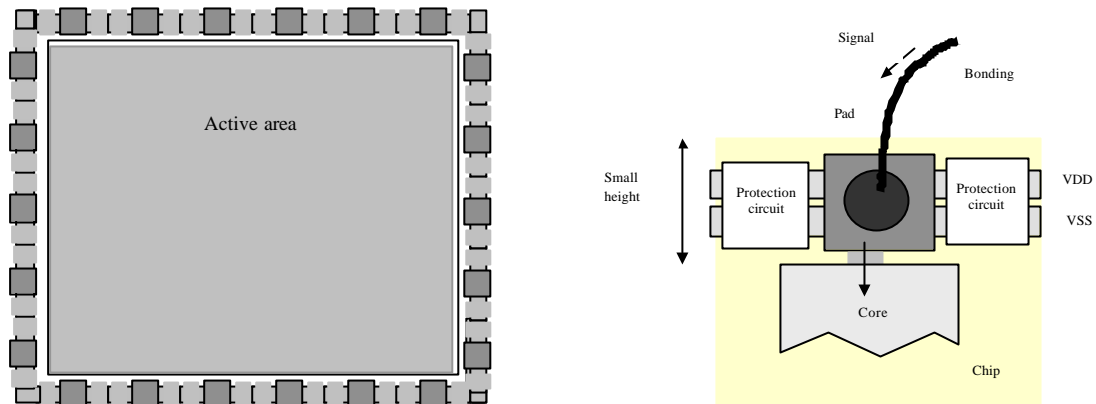


Fig. 10-4. Pads added to generate a pad ring around the chip.

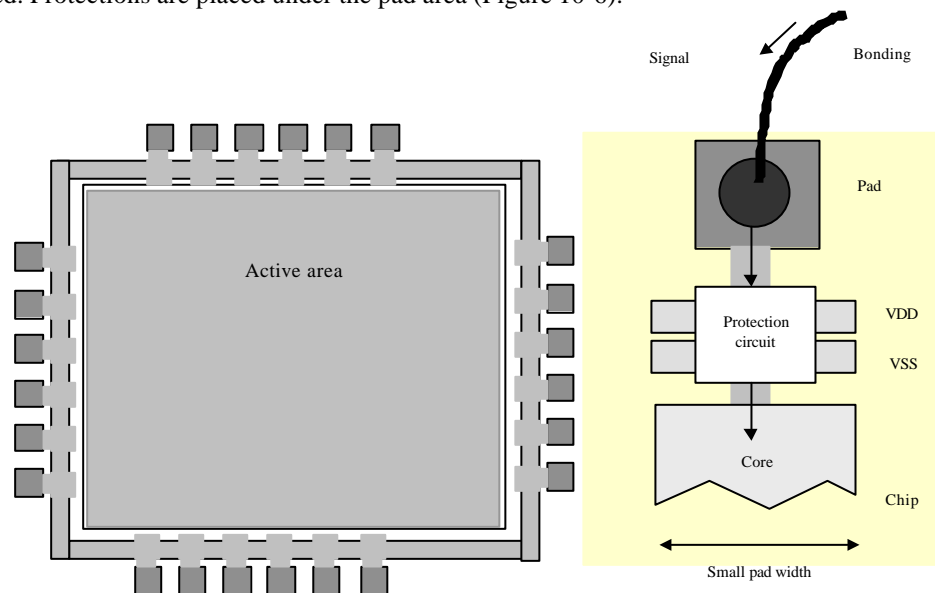


**CORE/PAD LIMITATION**

*Fig. 10-5 : chip size fixed by the core*

When the active area of the chip is the main limiting factor, the pad structure may be designed in such a way that the width is large but the height is as small as possible. In that case, the oversize due to the pads is minimized. Protections are placed on both sides of the pad area.

When the number of pads of the chip is the main limiting factor, the pad structure may be designed in such a way that the width is small but the height is large. In that case, the oversize due to the pads is minimized. Protections are placed under the pad area (Figure 10-6).



*Fig. 10-6. Pad limitation*

## ESD Protections

The input pad includes some voltage boosting and under voltage protections linked with problems of electrostatic discharge (ESD). Such protections are required as the oxide of the gate connected to the input could be destroyed by over voltage. One of the most simple ESD protection is made up of a set of two diodes and a resistance (Fig. 10-7). One diode handles the negative voltage flowing inside the circuit (N+/P substrate), the other diode (P+/N well) handles the positive voltage.

The layout of the N+/P\_Substrate diode includes a simple N+ diffusion in the P- substrate (the cathode K), surrounded by P+ contacts which polarize the P- substrate (the anode A). The current starts flowing between A and K if the voltage is roughly over 0.6V. In the reverse mode, the current is very small, in the order of some pico-Ampere. The polarization of the P- substrate is usually 0V. The diode N+/P- will be on if the voltage of the N+ region is less than -0.6V.

<to be added>

*Fig. 10\_7. Detail of the Input protection used against electrostatic discharge*