
B

Program Operation & Commands

Getting Started

To get your MICROWIND2 program started, use the following procedure:

- ❶ Insert the MICROWIND2 CD-Rom into drive
- ❷ Under Windows 95/NT, click on **Start -> Execute**
- ❸ Type **D:install** and press ↵
- ❹ Double click on the Microwind2 icon to start the software

The software runs on Windows 95, 98 and NT operating systems.



The command line may include two parameters:

1. The *First* parameter is the default mask file loaded at initialization
2. The *Second* parameter is the design rule file loaded at initialization

Example :

The command « **microwind2 fadd cmos018.rul** » executes MICROWIND2 with a default mask file « **fadd.MSK** » and the rule file « **cmos018.RUL** ». You may program the Microwind2 icon by a click with the right button, then “properties”.

List of Commands (*alphabetic order*)

About Information about the software release and contact for support.

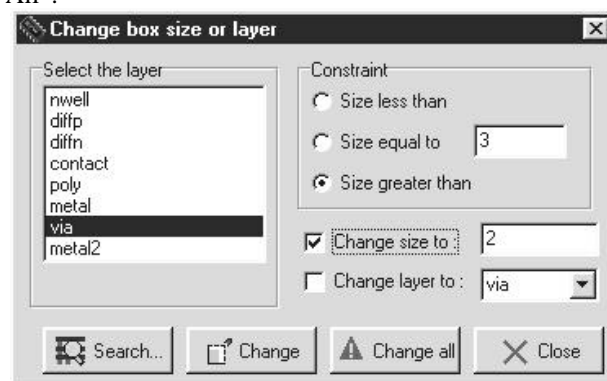
Microwind2

Add Text to Layout Use this icon to fix a text to one box or location in the design. That text illustrates the layout and should be used as much as possible for each significant node such as inputs and outputs. To add some text to a particular place, proceed as follows:



- ❶ Click on the icon
 - ❷ Set the text location with the mouse. A dialog box appears
 - ❸ Enter the text in front of “Label name:” and press “Assign”. The text is set in the drawing
- ◆ A text can be modified as follows: click on the icon, click inside the existing text. The old text appears. Modify it and click on “Assign”.
 - ◆ You may add a clock, a pulse, a VDD or VSS voltage source to the text.

Change Box Size or Layer This command is used for modifying boxes of a specific layer. A typical application is the reduction of all via from 3λ to 2λ . To do so, select the layer “via”, select the constraint “Size equal to 3”, select “Change size to” and finally click “Change All”.



- Colors**
- ◆ Switch to monochrome: the layout is drawn in black and white. This type of drawing is convenient to build monochrome documentation. Press “Alt”+“Print Screen” to copy the screen to the clipboard. Then, open “Word”, click “Edit-> Paste”. The screen is inserted into the document.
 - ◆ White background. The layers appear with a palette of colors on a white background.

Copy



Click on the *Copy* icon. Move the cursor to the design window, and delimit the active area with the mouse. Consequently, all the graphics included in this area are copied. The external shape of the copied elements appears. Fix those copied elements at the desired location by a click on the mouse.

Click on **Undo** to cancel the copy command.

Clean

Purge redundant boxes and overlapping boxes. This command is always invoked before simulation.

Layout

Cut



Click on the *Cut* icon. Move the cursor to the design window, and delimit the active area with the mouse.

Consequently, all the graphics included in this area are erased. Click on **Undo** to fix those elements back into the design.

- ◆ A layer is protected from erasing if you remove the tick in the palette twice. In the palette, an empty square to the right of the layer indicates a protected layer.
- ◆ A layer is unprotected from erasing if you select it again in the palette. A tick in the square to the right of the layer indicates an unprotected layer.
- ◆ One box only can be erased by a click inside that box when the cut command is active. The box is then erased.

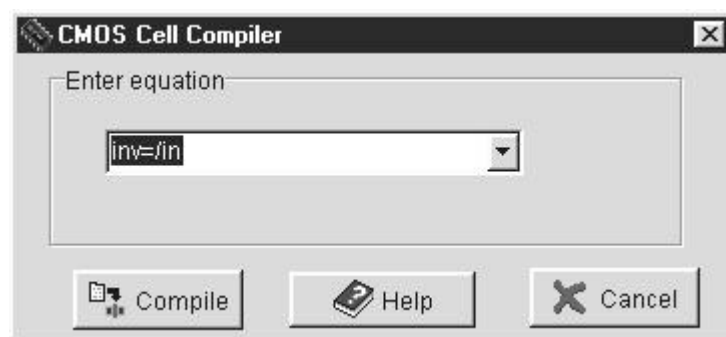
-

Compile

The cell compiler is a specific tool designed for the automatic creation of CMOS cells from logic description.

one Line

Click on **Compile** -> **Compile One Line**. The menu below appears. The default equation corresponds to a 3 input NOR gate. If needed, one can use the keyboard in order to modify the equation and then click on **Compile**. The gate is compiled and its corresponding layout is generated.



- ◆ The first item of the one-line syntax corresponds to the output name.
- ◆ The latter is followed by the sign « = », the optional sign not « / », and by the list of input names separated by the operators AND « . » or OR « . ». If need be, parenthesis can be added.
- ◆ The input and output names are 8 character strings maximum.

CELL	FORMULA
Inverter	$out = /in$
NAND gate	$n = /(a.b)$
3 Input OR	$s = a+b+c$
3 Input NAND	$out = /(a.b.c)$
AND-OR Gate	$cgate = a.(b+c)$
CARRY Cell	$cout = (a.b) + (cin.(a+b))$

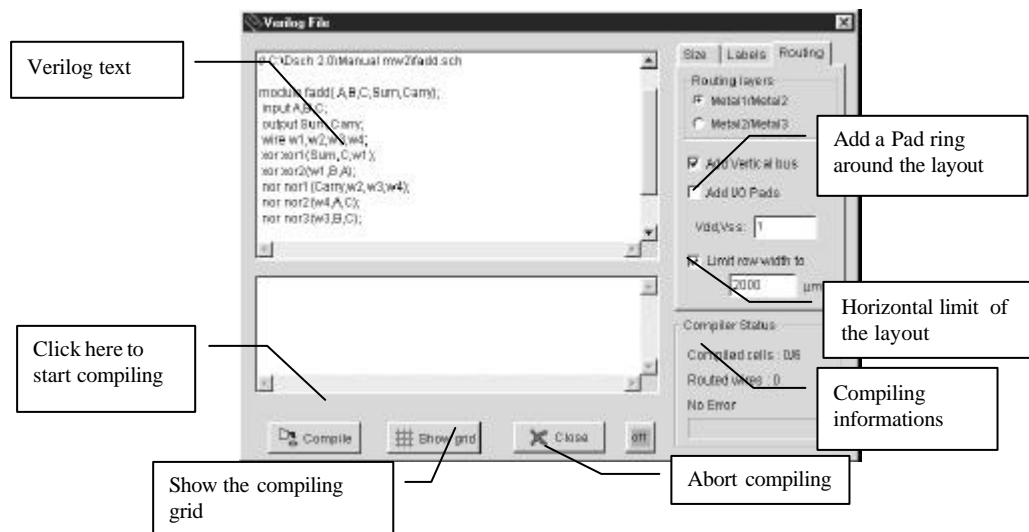
TRANSISTOR SIZE. The default device size is given by the design rules. You may change the nMOS and pMOS width in the option menu before clicking on PILE.

IMPLEMENTATION. The p-channel transistors are located on the top of the n-channel transistor net. If some layout already exists near those icons, the cell origin is moved to the right until enough free space is found. If the '/' operator has not been specified after the '=' sign, an inverter is added at the right hand side of the compiled cell. That is why an AND gate is compiled as a NAND gate followed by an inverter.

Compile The cell compiler can handle layout generation from a primitive-based VERILOG description text into a layout form automatically. Click on **Compile -> Compile Verilog File**. Select a VERILOG text file and click on **file** “Generate”. For instance, the **microwind2** directory contains the « FADD.TXT » file which corresponds to the description of a full-adder.

```
// Dsch 2.0a - 98 , Hierarchical Verilog
// 31/05/99 09 :23 :08
// C : \Dsch 2.0\Manual mw2\fadd.sch

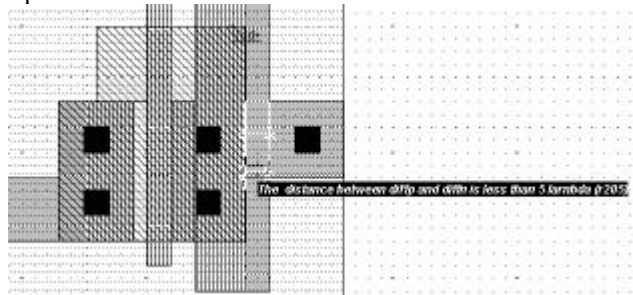
module fadd( A,B,C,Sum,Carry) ;
  input A,B,C ;
  output Sum,Carry ;
  wire w1,w2,w3,w4 ;
  xor xor1(Sum,C,w1) ;
  xor xor2(w1,B,A) ;
  nor nor1(Carry,w2,w3,w4) ;
  nor nor2(w4,A,C) ;
  nor nor3(w3,B,C) ;
  nor nor4(w2,B,A) ;
endmodule
```



PRIMITIVE	NODES	EXAMPLE
dreg	Inputs : Data, RESET, CLOCK Outputs: Q, nQ	dreg reg1(d,rst,h,q,nq);
Inv, not	Inputs : IN Outputs: OUT	inv inv1(s,e); // both 'inv' and 'not' not inv1(s,e); // can be used
and	Inputs : 2 to 4 Outputs: S	and and1(s,a,b,c,d); // limit inputs to 4
nand	Inputs : 2 to 4 Outputs: S	nand nand1(s,a,b,c,d);
or	Inputs : 2 to 4 Outputs: S	or or3(s,a,b,c);
nor	Inputs : 2 to 4 Outputs: S	nor my_nor4(s,a,b,c,d);
xor	Inputs : a,b Outputs: S	xor xor_gate(xor_out,d0,d1);
Nmos	Inputs: gate, source Outputs: drain	nmos nmos1(d,s,g);

Design**Rule****Checker**

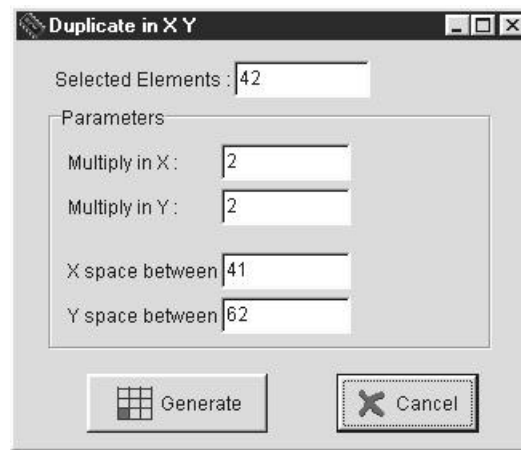
The design rule checker (DRC) scans all the design and verifies that all the minimum design rules are respected. Click on the icon above or on **Analysis ->Design Rule Checker** to run the DRC. The errors are highlighted in the display window, with an appropriate message giving the nature of the error. Details about the position and type of the errors appear on the screen. To obtain any further information about the design rules, see Chapter 8.

**Draw a****Box**

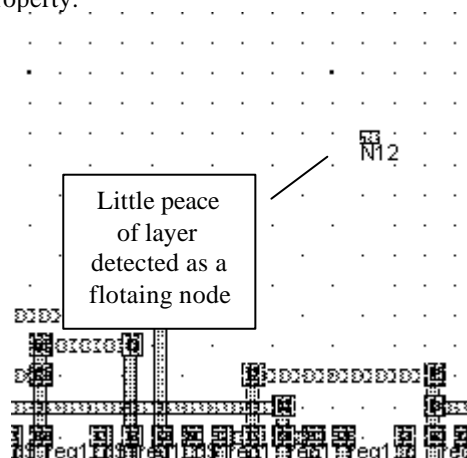
The « Draw Box» icon is the default icon. It creates a box in the selected layer. The default layer is polysilicon. If the « Draw Box » icon is not selected, click on it. Then, move the cursor to the display window and fix the first corner of the box with a press of the mouse. Keep pressed and drag the mouse to the opposite corner of the box. Release the mouse and see how the box is created.

- ◆ The active layer is selected in the palette.
- ◆ The red color indicates the active layer.
- ◆ The tick specifies that all boxes using the layer can be erased, stretched or copied.
- ◆ Removing the tick protects the layer.

Duplicate XY The command « Duplicate XY » is very useful to generate an array of identical cells such as RAM cells for example. Click on **Edit -> Duplicate XY**, include the elements to duplicate in an area defined by the mouse, and the following screen appears. In both X and Y, the default multiplication factor is x 2. You may adjust the space between cells. By default, the cells touch each other. Selected boxes appear in yellow on the screen.

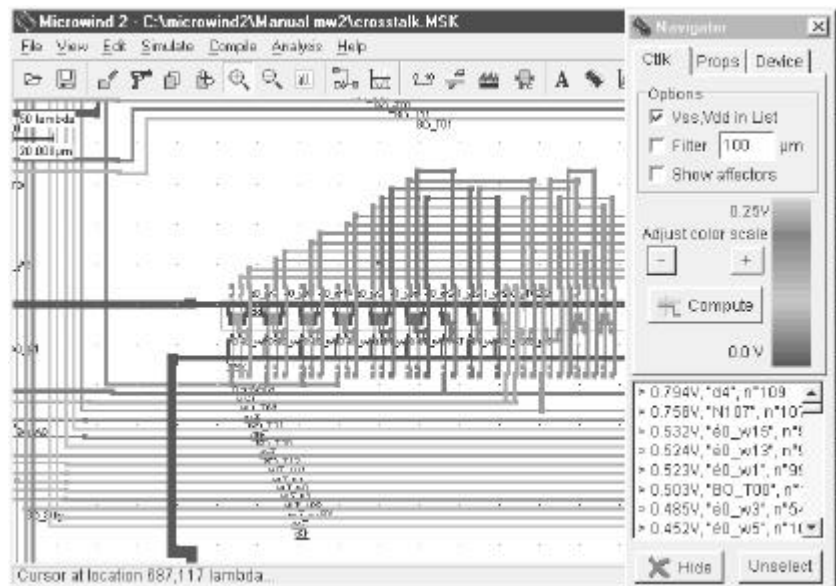


Find floating nodes Click on **Analysis -> Find Floating Nodes** to scan the layout and detect nodes that might be floating. The navigator gives the list of the floating nodes in the Navigator menu. Click on the corresponding name to locate it in the drawing. A floating node is an interconnect not connected to a diffusion. Floating gates are listed even if they include a clock or pulse property.



Flip To apply a rotation or a flip to one part of the design, click on **Edit -> Flip <->**. Delimit the active area of the boxes in the layout so that it can be modified using the mouse.

Global Crosstalk Click on **Analysis -> Global Crosstalk** to scan the layout and detect nodes with high level of crosstalk noise. The navigator gives the list of nodes with decreasing sensitivity to crosstalk noise. Click on the corresponding name to locate it in the drawing. See chapter 11 for more information about the origin of crosstalk noise.



Help Provides an on-line help for using Microwind2. Includes a summary of commands.


Insert The command **File -> Insert** is used to add a MSK file to the existing files. The inserted layout is fixed at the right lower side of the existing layout. The current file name remains unchanged.

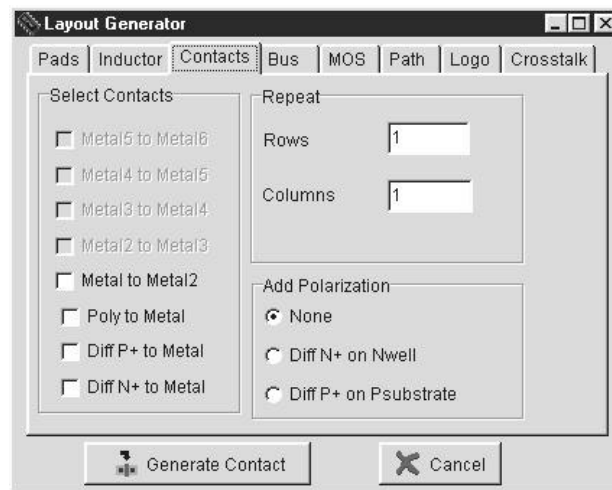
Leave Microwind2 Click on **File -> Leave Microwind2** in the main menu. If you have made a design or if you have modified some data, you will be asked to save it. After confirmation, you can return to Windows.

Library

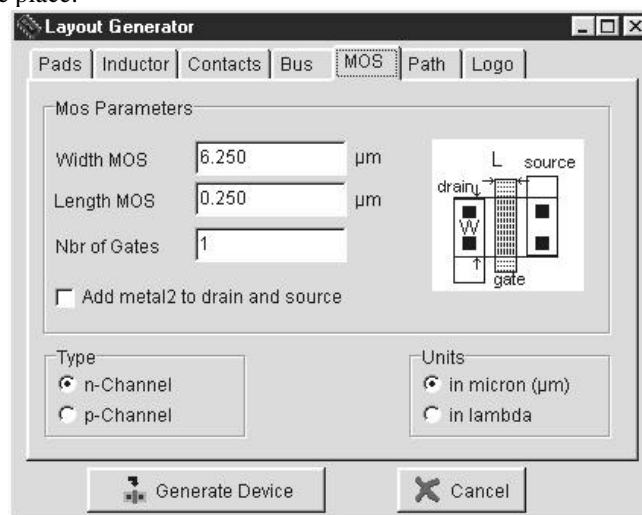


The library contains a set of predefined layout macros such as contacts, devices and pads. Those cells are built according to design rules, and contain size parameters. To invoke the cell library click on the above icon.

- ◆ CONTACTS such as polysilicon/metal, n-diffusion/metal, p-diffusion/metal and metal/metal2 metal2/Metal3,(etc...), or stacked contacts can be obtained here. You may also click the icon in the palette . Multiple contacts can be generated when entering number of contacts in X and Y greater than one. You may also generate a polarization seal around the contact to create a pad diode protection for example.



- ◆ MOS. This macro generates either a n-channel or a p-channel transistor. The parameters of the cell are the channel length (default value is given by the design rules), its width, and the number of gates. Once those parameters are defined, the device outline appears. Click on the mouse to place it in the appropriate place.



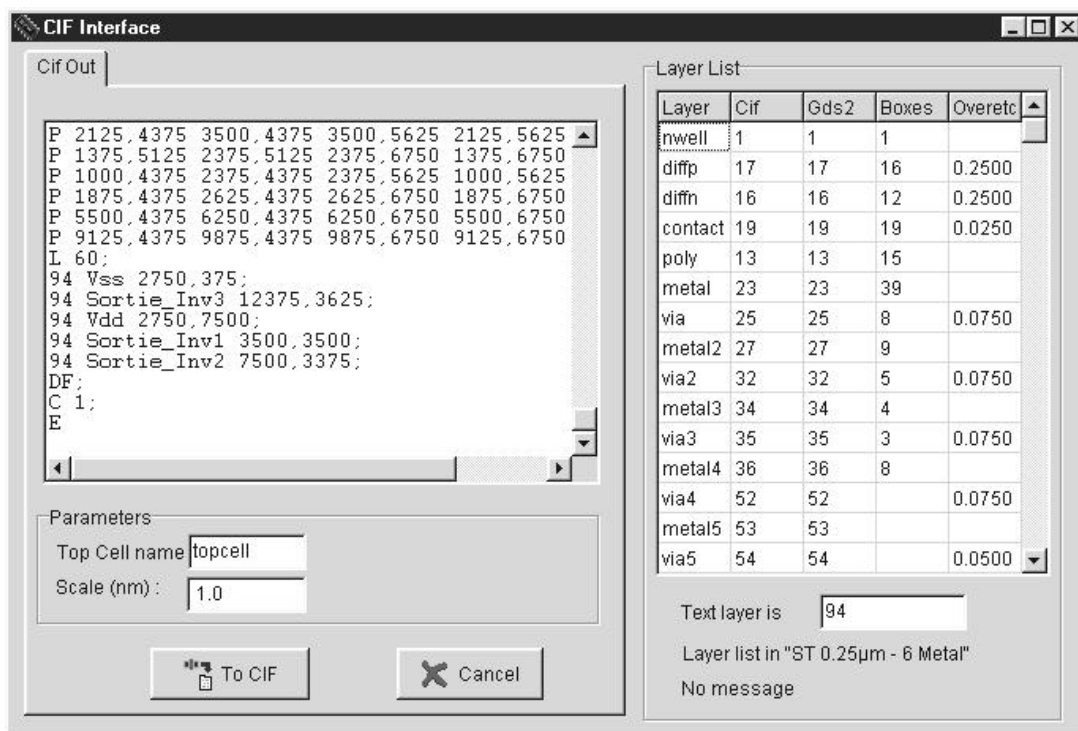
- ◆ PADS. It is possible to add various items such as a single pad, a test pad (usually 30x30 μm), or even a set of pads all around and to the layout using the VDD and VSS power rings. In the last case (adding more than one pad), give the number of pads each side of the chip and if need be modify the width of the VDD and VSS tracks, as well as the number of VDD/VSS pad pairs.
- ◆ PATH. This command generates a path of interconnects using one single layer. The path width can be changed, as well as the alignment to the routing grid. A set of contacts can also be placed at both ends of the path. This command is very useful for VDD and VSS supply drawing and single layer interconnects.
- ◆ BUS. This command generates a set of parallel lines with user-defined layer, width and spacing. This command is useful to build coupled interconnects, or bus path used in the final routing of a chip.

- ◆ **INDUCTOR.** This command generates a coil made from use-defined metal layers. This item is used for very-high frequency oscillators. In MICROWIND2, this inductor is viewed as a simple interconnect as it does not handle inductance.

Make Cif File

MICROWIND2 converts the MSK layout into CIF using a specific interface, invoked by “**File -> Make CIF file**”. The CIF file can be exported to VLSI CAD software. The right table of the screen gives the correspondence between MICROWIND2 layers and CIF layers, the number of boxes in the layout and the corresponding over-etch. The overetch is used to modify the final size of the CIF boxes in order to fit the exact design rules.

- ◆ Click on « **Convert to CIF** » to start conversion. Some parts of the result appear in the left window
- ◆ The main unit is 1nm. You may change it to fit the requirements of the target CAD tool.
- ◆ For CMOS 0.25µm rule file (cmos025.RUL), notice the overetch applied to contact and via. This overetch is mandatory to obey the final design rules, while keeping the user-friendly and portable lambda-based design.



Make Spice File

Click on **File -> Make Spice File** to translate your design into a SPICE compatible description. The circuit extractor included in the software generates the equivalent circuit diagram of the layout and a spice compatible netlist ready to be simulated. You may select the model you will be using for simulation. The choice lies between model 1, model 3 and model 9.

- ◆ The SPICE description includes the list of n-channel and p-channel transistors and their associated

width & length extracted from the layout.

- ◆ The text file also details the node names, parasitic capacitances, and device models.
- ◆ The SPICE filename corresponds to the current filename with the appendix **.CIR**

Measure distance



The ruler gives the horizontal and vertical measurements (dx and dy) between two points, directly on the screen in lambda and in micron. The algebraic distance (d) is also given in μm . The ruler is simply erased by the command **View -> Refresh the screen** or by a press of <ESC>.

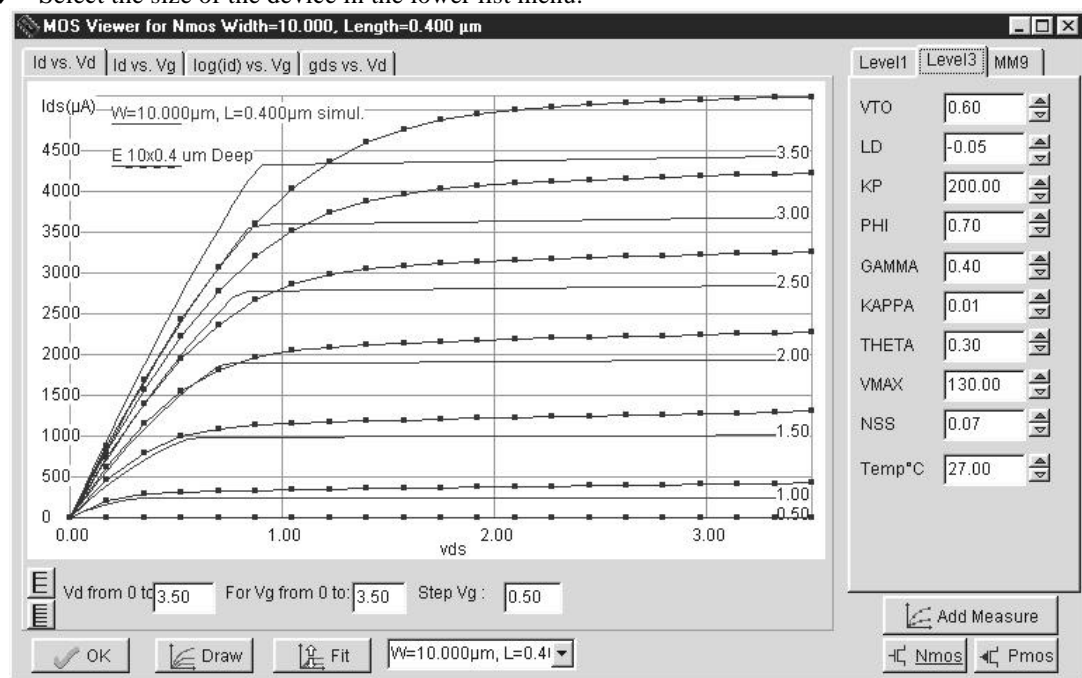
MOS

Click on the icon. The Id/Vd curve of the default MOS ($W=20\mu\text{m}$, $L=L_{\text{minimum}}$) appears.

Characteristics



- ◆ The effects of the changing of the model parameters can be seen directly on the screen by a click on the little arrows (Up/down), which change the parameter values.
- ◆ Click “Id vs. Vg” to highlight the threshold voltage
- ◆ Click “Id(log) vs. Vg” to see the sub-threshold behavior.
- ◆ Add measurements by selecting a « .MES » file
- ◆ Skip from NMOS to PMOS device by a click on the corresponding button
- ◆ Select the size of the device in the lower list menu.



Three models can be used :

- MOS Model 1 (Berkeley Spice)
- MOS Model 3 (Simplified version of Berkeley Spice)
- MOS Model 9 (Almost complete version of Philips MM9 model)

MOS List

Click “Edit -> MOS List” to get the list of n-channel and p-channel MOS devices currently edited in the layout. The MOS list is displayed in the navigator window. Click the desired MOS in the list to zoom at the corresponding location in the layout.

Move,***Stretch a Box***

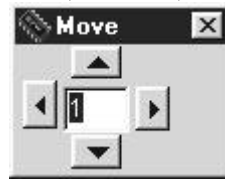
To move one box, click on the above icon. Using the mouse, create an area that includes the box. Then, drag the mouse to the new location and release the mouse. As a result, the box has been moved the new place. Repeat the same in order to move a set of boxes.

- ◆ To protect a layer from moving, click in the rectangle the palette that is situated on the right side of the layer. This will remove the tick.
- ◆ To stretch a box, click on one side of the box that you want to stretch. The box outline appears. Drag the mouse to the new location and release the button. The box is stretched.

TIP: To catch the desired border of the box, draw a line perpendicular to the border, entering the box.

Move

To move one box lambda per lambda, click “Edit -> Move Step by Step”. Using the mouse, create an area that includes the boxes. The selection appears in yellow. Then, click the arrow until the selection has been moved the new place. The step value (in lambda) is fixed in the edit line.

**New**

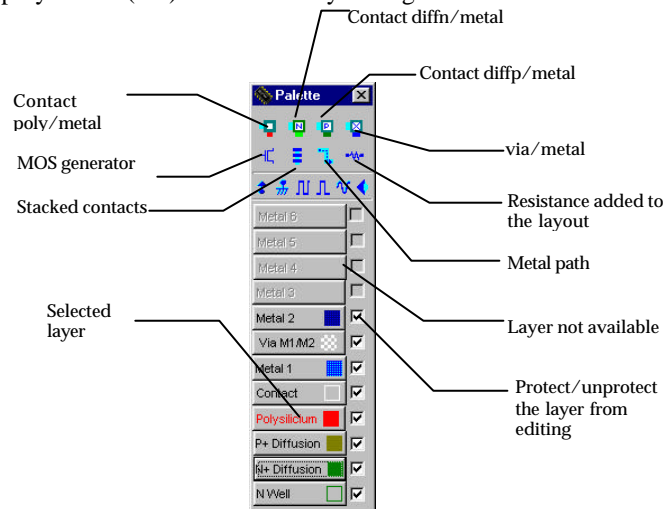
Click on **File-> New** in order to restart the software with an empty screen. The current design should be saved before asserting this command, as all the graphic information will be physically removed from the computer memory. No **Undo** is available to disable the **New** command.

Open

Click on the above icon. In the list, double-click on the file to load. « .MSK » is the default extension that corresponds to the layout files. The CIF files « .CIF » can also be loaded. The appropriate conversion program transforms the input CIF into MSK format.

Palette

The palette is located on the right side of the screen. A little tick indicates the current layer. The selected layer by default is a polysilicon (PO). The list of layers is given below.



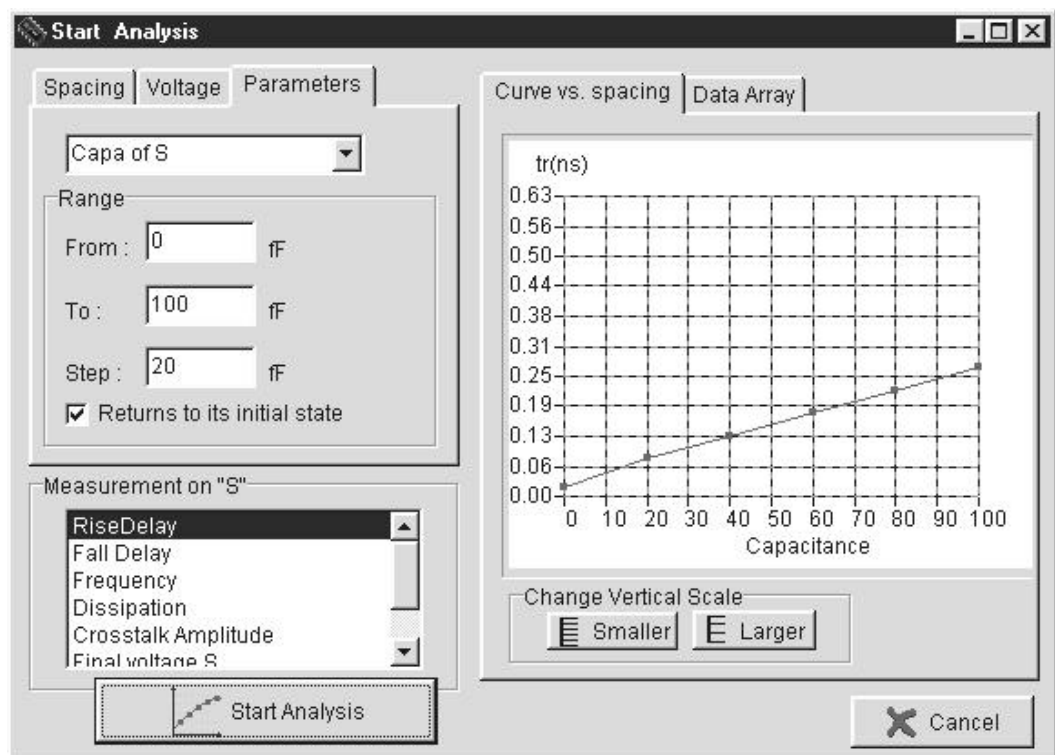
- ◆ If you remove the tick on the right side of the layer, the layer is switched to protected mode. The Cut, Stretch and Copy commands no longer affect that layer.
- ◆ Use “View->Protect all” to protect all layers. The ticks are erased.
- ◆ Use “View->Unprotect all” to remove the protection. All layers can be edited.

Parametric Analysis

Before running the parametric analysis, you should run a simulation first. Select the desired output node on which the delay measurement or frequency measurement is performed, then click on **Analysis -> Parametric Analysis**. Click on a cell output node in the layout. The window below appears. The parametric analyzer allows you to easily investigate the influence of various parameters on the cell performance.

- ◆ In the parameter menu, you may investigate the influence of temperature, power supply or that of a node capacitance.
- ◆ In the measurement menu you may choose to monitor the rise and fall delay, the power consumption, or the frequency.

Click on «**Start Analysis** ». An iterative procedure will conduct simulations and extract the relevant parameters. The result below shows the evolution of the cell delay when its output node capacitance has been changed. Notice that for high capacitance values, the cell response is very slow. The input clock parameters should be consequently be adjusted in order to fit with low speeds.



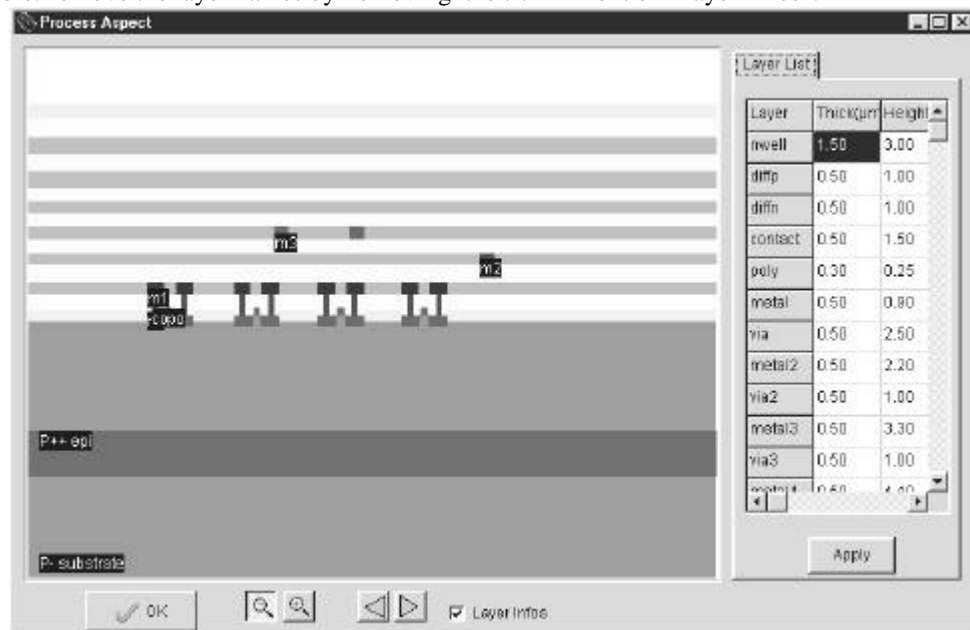
Prediffusion Mode

In that mode, diffused layers are no more accessible. Only upper layers (metal and via) can be added to the layout.

Process Section in 2D

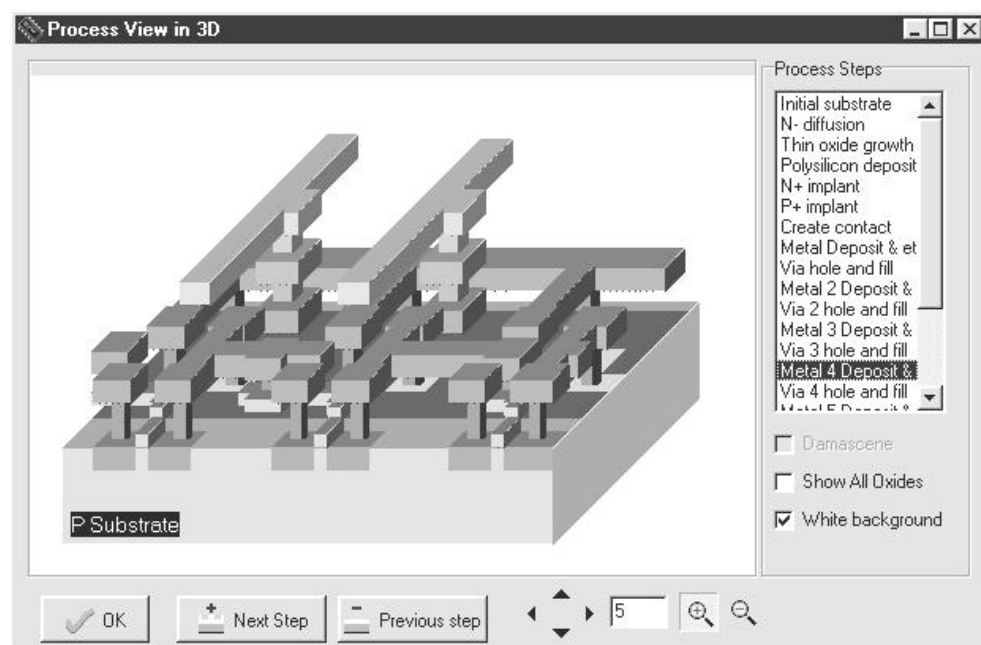
Click on the above icon to access process simulation. A mouse-operated line is given and embodies the cross section. The screen below appears. The arrows can be used to move the cross-section to the right or to the left in the X axis, and forward and backward in the Y axis. Zooms in and out are

available. Remove the layer names by removing the tick in front of “Layer infos”.



Process Section in 3D

Click “Simulation -> Process Steps in 3D”. Click “Next step” to watch how the layout currently edited on the screen will be fabricated using the selected technology. Use the arrow to shift the displayed portion. Zooms in and out are available.



Protect All

Click on “View ->Protect All” to protect all layers for editing purpose. All ticks in the palette are removed.

Print Layout

Click on **File ->Print Layout** to transfer the graphical contents of the screen to the printer.

Alternatively, you can make a copy of the window into the clipboard in order to import the screen into your favorite text editor by pressing <Alt>+<Print Screen>. In the text editor or in the graphic editor, simply click on « Edit ->Paste » We recommend that you switch to monochrome mode first by invoking

the function **File -> Colors -> Switch to Monochrom**. In that case the layout will be drawn in a white background color using gray levels and patterns.

Rotate

To apply a rotation to one part of the design, click on **Edit -> Rotate**. Delimit the active area of the boxes in the layout so that it can be modified using the mouse.

Save

Click on **File -> Save** to save the layout with its current name. The default name is « EXAMPLE.MSK »

Save As

A new window appears, into which you are to enter the design name. Use the keyboard and type the desired file name. Press « Save ». Your design is now registered within the **.MSK** appendix.

Search Text

The most convenient way to find a text in the layout is to invoke **Edit -> Search text**. The list of text labels appears in the navigator menu. If you click on the desired text, the screen is redrawn so that the text label is at the center of the window, with two lines drawing a cross at the text location. Its properties appear in the navigator menu.

- ◆ Click on **Hide** to close the navigator window.
- ◆ Click on **Extract** to add the electrical properties of the selected text if the layout has not been previously extracted.
- ◆ In the case of a very long text list, select the first letter of the text at hand, press that letter on the keyboard. This will automatically effect an alphabetic search and the selector will move to the first label starting with the selected letter.

Select Foundry

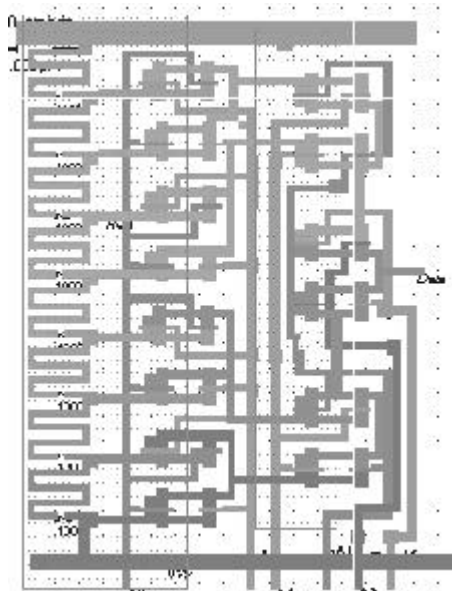
Click on **File -> Select Foundry**. The list of available processes appears. The default design rule file is written in bold characters. Various technologies are available from 1.2 down to 0.12 μm . Click on the rule file name and the software reconfigures itself in order to adapt to the new process

Simulation***Parameters***

- ◆ The default extraction includes the removal of redundant boxes (Purge) and the removal of overlaps (Merge). The fast extraction does not handle Purge nor Merge operations.
- ◆ The MOS level can be chosen between level 1,3 and 9. See chapter 2 for more details about those models.
- ◆ Other options concern the computation of lateral capacitance and vertical crosstalk capacitance

Simulation on layout

The simulation is performed directly on the layout with a palette of colors. The most interesting layout files to be simulated in this mode are analog blocks such as the DAC.

**Start Simulation**

The above icon or the command **Simulate -> Start Simulation** both give access to the automatic extraction and analog simulation of the layout.

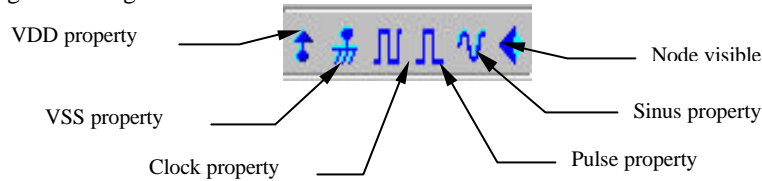
- Click on **Voltage vs Time** to obtain the transient analysis of all visible signals. The delay between the selected **start node** and selected **stop node** is computed at $VDD/2$. You can change the selected **start node** in the node list, in the right upper menu of the window. You can do the same for the selected **stop node**.
- Click on **Voltage and Currents** so as to make all voltage curves appear in the lower window, and the VDD, the VSS and the desired MOS currents appear in the upper window. In that mode, the dissipated power within the simulation is also displayed.
- Click on **Voltage vs. Voltage** to obtain transfer characteristics between the X-axis selected node and the Y-axis selected node. Initially the start node is the first clock or pulse of the node list, and the stop node is the first varying node. This mode is useful for the computing of the Inverter characteristics (commutation point), the DC response of the operational amplifier, or for the Schmitt trigger to see the hysteresis phenomenon. The first simulation computes the value of the **stop node** for **start node** varying from 0 to VDD. The second click on « Simulate » computes the same for **start node** varying from VDD to 0.

NOTE : You can modify the minimum simulation step Δt , but it may be dangerous. If you increase Δt the simulation speed improves but the numerical error may lead to unstable simulations. If you decrease Δt , the simulation speed is decreased too but the numerical precision is improved. The risk of computing divergence is reduced.

Simulation Icons

The simulation icons add **properties** to the nodes. Properties are applied to the electric nodes of the circuit in order to serve as simulation guides. You must specify which node is assigned to which voltage

before starting the analog simulation.



VDD & VSS. The node is pushed to the power supply voltage with icon *Vdd*, and pulled to the ground 0V with icon *Vss*.

CLOCK. When a node becomes a clock, the parameters of the latter are divided as follows : rise time, level one, fall time, and level zero. All values are expressed in nan-second (ns). If you ask for a second clock, the period will be multiplied by two.

- ◆ You may alter **level 0** and **level 1** by entering a new value with the keyboard.
- ◆ To generate a clock starting from VDD instead of VSS, click on **Invert L/H**
- ◆ Use **Period * 2** to multiply the clock period by two.
- ◆ Use **Period /2** to divide the clock period by two.

PULSE. The pulse switches from “Level 0” (0 by default) to “Level 1” (VDD by default” depending on the user-defined time table.

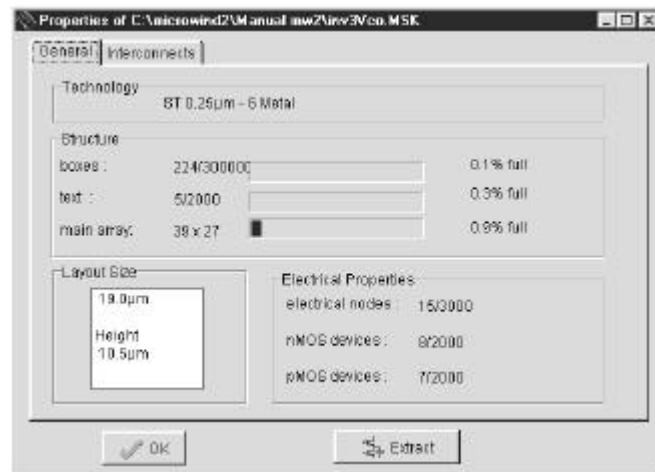
- ◆ Enter the string “0101100” and press “Insert”. The time-table is updated
- ◆ Click “Erase”: all lines situated after the selected element of the time-table are erased.

SINUS. The sinusoidal waveform parameters are the amplitude, the offset, frequency and phase.

VISIBLE NODE. Click on the “eye” and click on the existing text in the layout to make the chronograms of the node appear. Initially, all nodes are invisible, but the clocks and impulse nodes are subsequently made visible.

Statistics

The command **File -> Statistics** provides some information about the current technology, the percentage of memory used by the layout and the size of the layout plus its detailed contents. If the layout has previously been extracted or if you click « **extract now** », the number of devices and nodes will be updated.

**Undo**

The Undo command (**Edit -> Undo**) is useful to not take into account the last editing command. It is possible to undo the commands Cut, Paste, Copy, Move, Stretch, Edit and Compile.

Unprotect All

Click on “View ->Unprotect All” to select all layers for editing purpose. All ticks in the palette are asserted.

Unselect All

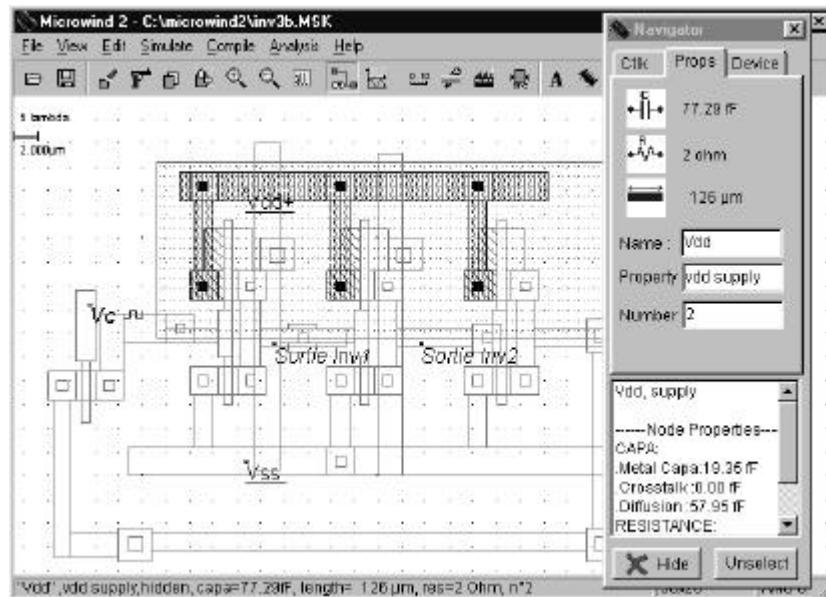
Click on **View -> Unselect All** (or <ESC>) to unselect the layout. This command is useful to draw the layout back into its default colors after commands such as **View Interconnect** or **View Node** which highlight one single node.

View All

Click **View -> View All** to fit the screen with all the graphical elements currently on display.

View Node

Click on the icon above or on **View ->View Node**. Then, click in the desired box in the layout. After an extraction procedure has been carried out, you will see that all the boxes connected to that node. In the case of a large layout, the command may take time. The associated parasitic capacitance, the list of text labels added to the selected boxes, and the node properties are also displayed in a separate navigator window. Click “Unselect”, “Hide”, <Escape> or **View -> Unselect All** to unselect the layout.



View Interconnect

The command **View -> View Interconnect** performs an electrical extraction of the metal and polysilicon boxes connected to the desired point. Compared to **View Node**, this command works faster but does not consider diffused layers that can extend the node interconnect network. The command gives the list of connected text labels.

Click on <Escape> or on **View -> Unselect All** to unselect the layout.

Zoom In & Out



The above icons perform **Zoom In** and **Zoom Out**. When zooming in, the area determined by the mouse will be enlarged to fit the display window. When zooming out, the area determined by the mouse will contain the display window.

- ◆ If you click once, a zoom is performed at the desired location.
- ◆ Press **Ctrl+A** for « **View All** », and **Ctrl+o** for zoom out.