

3

The Inverter

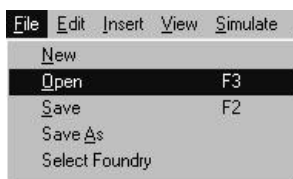
This chapter describes the CMOS inverter at logic level, using the logic editor and simulator DSCH2, and at layout level, using the tool MICROWIND2.

1. THE LOGIC INVERTER

In this section, an inverter circuit is loaded and simulated.



① Click on the icon above to activate the Dsch2 software.



② Click *File* → *Open* in the main menu. Select “INV.SCH” in the list. In this circuit are on button situated on the left side of the design, namely A, an inverter and a led.

③ Click *Simulate* → *Start simulation* in the main menu.

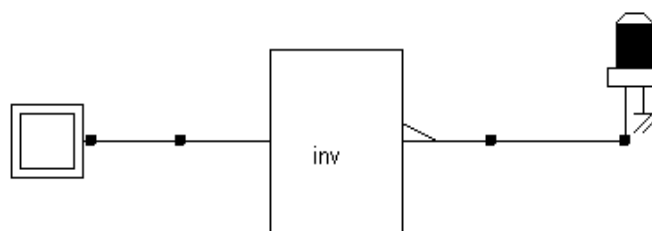
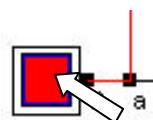


Fig. 3.1: The schematic diagram including one single inverter (Inverter.SCH)



④ Now, click inside the buttons situated on the left part of the diagram. The result is displayed on the lamps. The red value indicates logic 1, the black value means a logic 0.



⑤ Click the button “Stop simulation” shown in the above picture. You are back to the editor.



© Click the above icon to get access to the chronograms of the simulation.

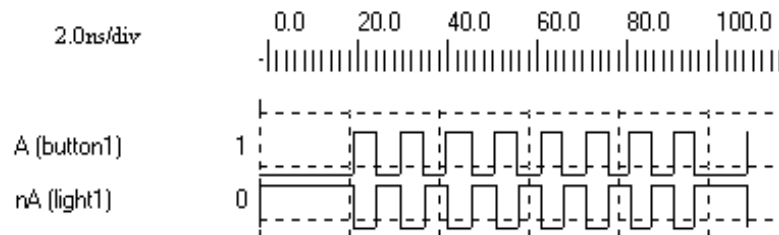


Fig. 3.2: Chronograms of the inverter simulation (*Inverter.SCH*)

Double click on the INV symbol, the symbol properties window is activated. In this window appears the VERILOG description (left side) and the list of pins (right side). A set of drawing options is also reported in the same window. Notice the gate delay (0.06ns in the default technology), the fanout that represents the number of cells connected to the output pin (1 cell connected), and the wire delay due to this cell connection (An extra 0.1ns delay).

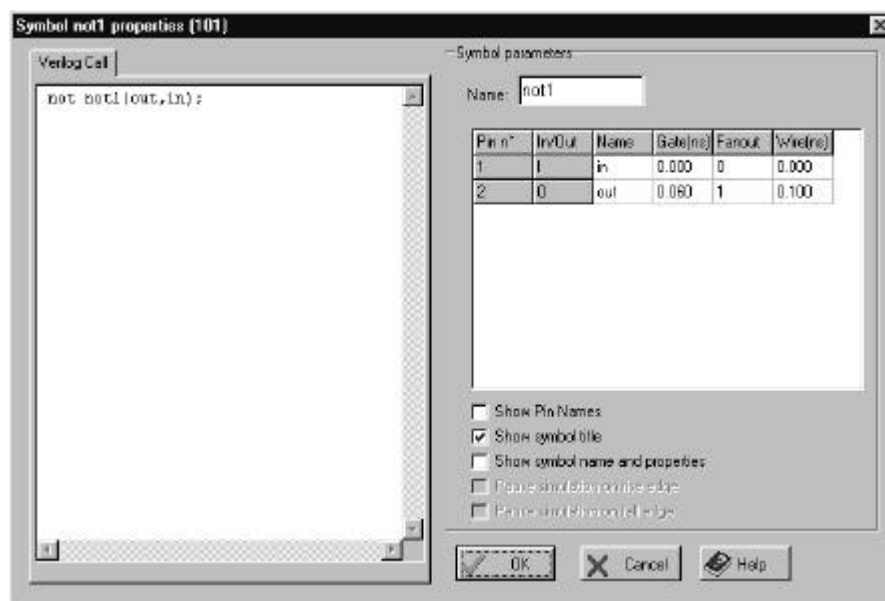


Fig.3.3 Symbol properties window

2. THE CMOS INVERTER

The CMOS inverter design is detailed in the figure below. Here the p-channel MOS and the n-channel MOS transistors function as switches. When the input signal is logic 0 (Fig. 3.4 left), the nMOS is switched off while PMOS passes VDD through the output. When the input signal is logic 1 (Fig. 3.4 right), the pMOS is switched off while the nMOS passes VSS to the output.

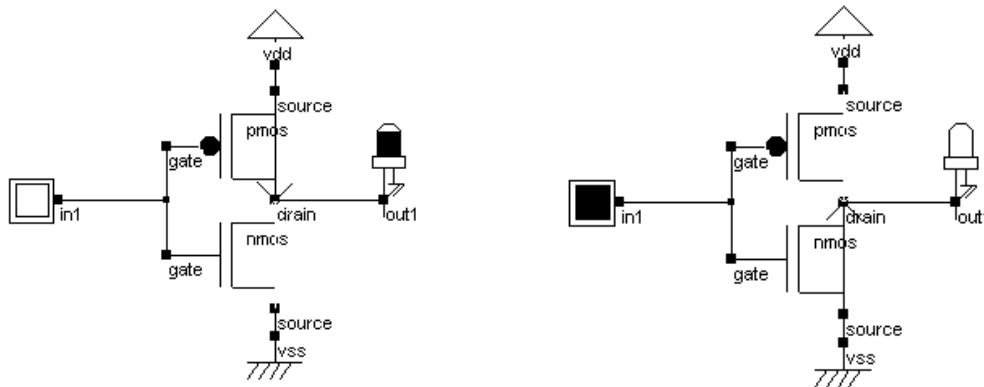


Fig. 3.4: The MOS Inverter (File CmosInv.sch)

Introduction to Power consumption

The inverter consumes power during transitions, due to two separate effects. The first is short circuit power arising from momentary short-circuit current that flow from VDD to VSS when the transistor functions in the incomplete-on/off state. This state occurs briefly during transitions of the output, either from 0 to 1 or from 1 to 0 (Fig. 3.5).

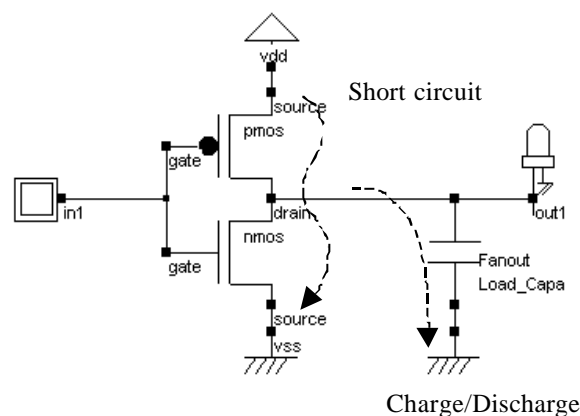


Fig. 3.5: Short circuit current in CMOS inverters

The second is the charging/discharging power, which depends on the output wire capacitance. With small loading, the short circuit current is dominant. But as the number of gates connected to the inverter

increase, the load capacity increases. Consequently, the charging and discharging current starts to dominate the short circuit current.

Fanout effect

The fanout corresponds to the number of gates connected to the inverter output. Physically, a large fanout means a large number of connections, that is a large load capacitance. An inverter circuit is simulated using different clock, fanout and supply conditions. The initial configuration is a 100MHz clock, one output connected to the inverter and a supply voltage 2.5V. To investigate the fanout effect on the consumption, we simulate first the inverter with one single output. In the simulation chronograms, we observe that 0.018 mW with a fanout 1. The corresponding file is FANOUT1.SCH.

Now, we add other lights to the output node, thus increasing the charge capacitance. In the simulation chronograms, both the inverter delay and the power consumption have increased (0.059 mW with a fanout of 4). The power consumption linearly increases with the load capacitance. This is mainly due to the current needed to charge and discharge that capacitance. The corresponding file is FANOUT4.SCH

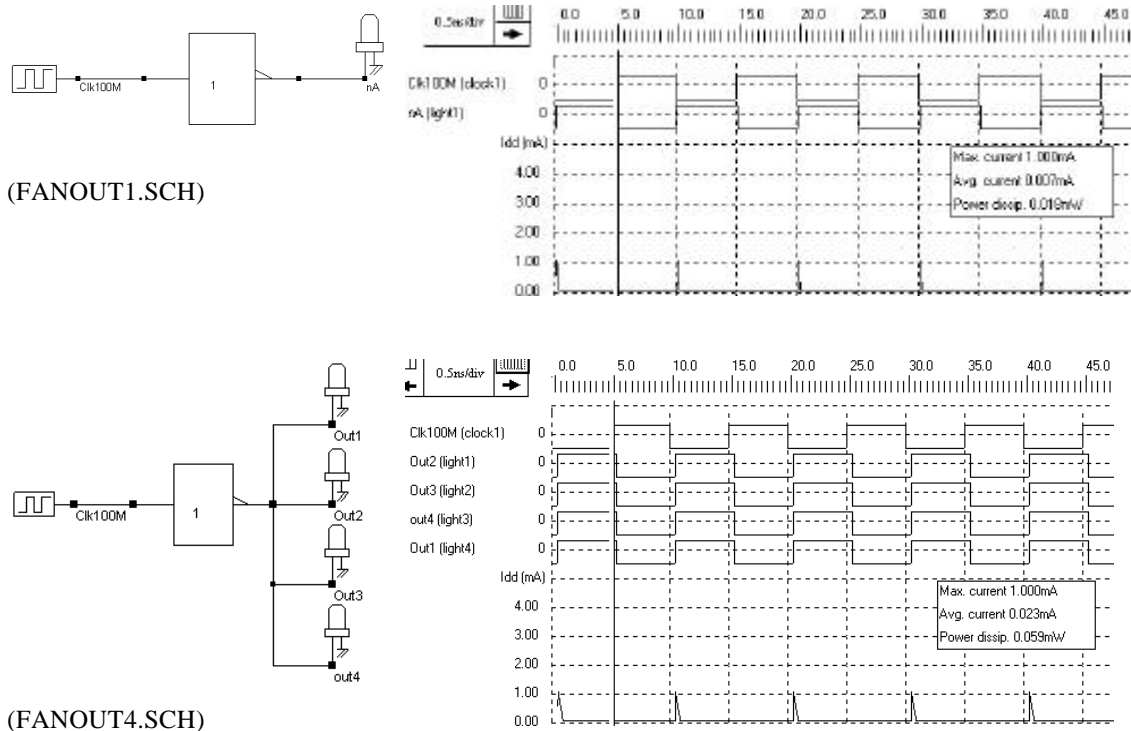


Fig. 3.6: Power consumption increase with the fanout (Fanout1.SCH and Fanout4.SCH)

Frequency effect

Now we simulate the CMOS inverter circuit with different clock frequency, keeping a constant fanout. The power consumption increases linearly with the clock frequency, as can be observed by changing the internal parameters of the clock symbol and watching the resulting power dissipation. In the case of 3.7, a 500MHz switching of the inverter consumes 5 times more power than a 100MHz switching.

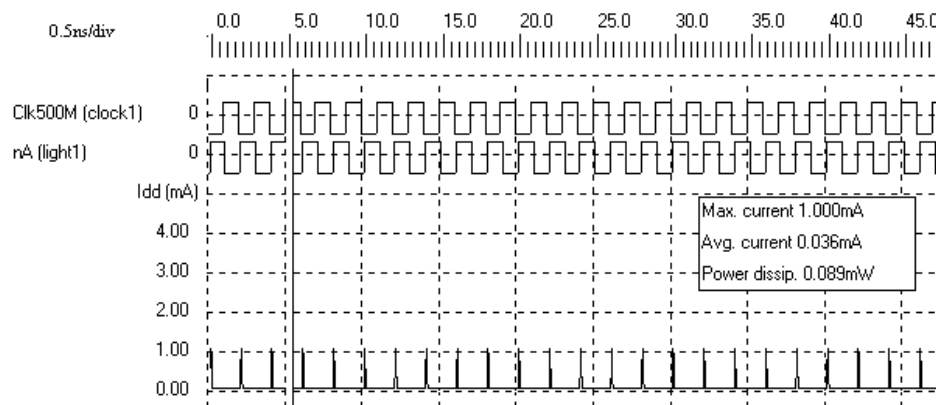


Fig. 3.7: Power consumption increase with the operating frequency (*Fanout1Fast.SCH*)

Supply voltage effect

We may configure the software with a 5V technology (AMS08.TEC), using the command “File -> Select Foundry”. With VDD=5V, the same circuit at the same speed consumes 0.754mW, that is more than 10 times the consumption with a 2.5V technology. It can be considered, as a first-order approximation that the average power consumption is proportional to VDD^2 .

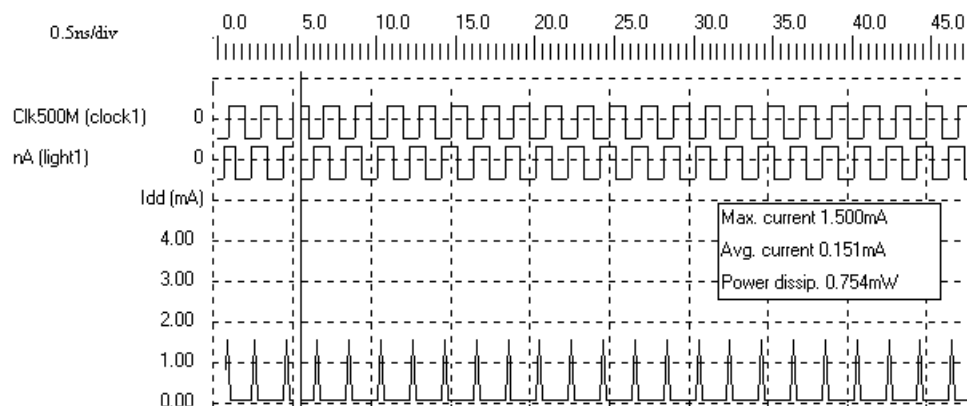


Fig. 3.8: Power consumption decrease with VDD (*Fanout1Fast.SCH*)

In summary, three factors contribute to the power consumption: the load capacitance C , the supply voltage VDD and the clock frequency f . For a CMOS inverter, this relation is represented by the equation below. The equation remains valid for more complex gates, although some extra considerations have to be taken into account.

$$P = k C VDD^2 f$$

Where:

k : technological factor (close from 1)

C : Output load capacitance (Farad)

VDD : supply voltage (V)

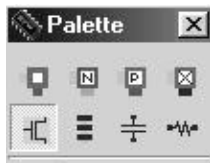
f : Clock frequency (Hz)

3. MANUAL LAYOUT OF THE INVERTER

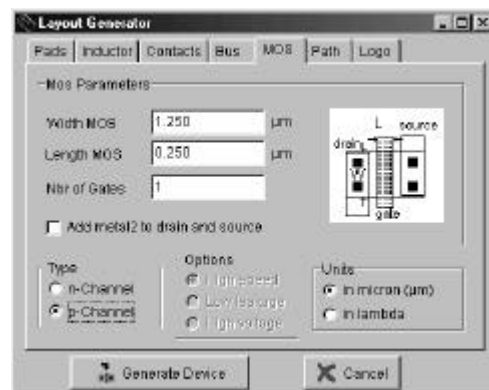
In this paragraph, the procedure to create manually the layout of a CMOS inverter is described.



① Click on the icon above to activate the Microwind2 software.



② Click the icon “MOS generator” on the palette. The following window appears. The proposed size is $1.25\mu\text{m}$ for the width, $0.25\mu\text{m}$ for the length. Simply click “Generate Device”, and click on the middle of the screen to fix the MOS device.



③ Click again the icon “MOS generator” on the palette. Change the type of device by a tick on “p-channel”, and click “Generate Device”. Click on the top of the nMOS to fix the pMOS device. The result is displayed in figure xxx.

+++++++ ETIENNE ++++++

Fig.3.xxx nMOS and pMOS devices placed on the layout

<Draw nMOS, draw pMOS>

<Same siez with MOS generator>

<Transcient>

<Add load with C>

<V/V is non symettrical>

<Change Wp to have symmetry>

4. COMPILE THE INVERTER INTO LAYOUT

An alternative to manual layout is the automated layout, also called “silicon compilation”. In this paragraph, the procedure to create automatically the layout of a CMOS inverter from its high level description is described. Click the command *File* → *Make Verilog File*. A new window appears. The content of the text file «Inverter.TXT» is reported in the editing window. It corresponds to the VERILOG description of the circuit “Inverter.SCH”. The primitive ‘NOT’ appears in the text. Click “OK” to close the window.

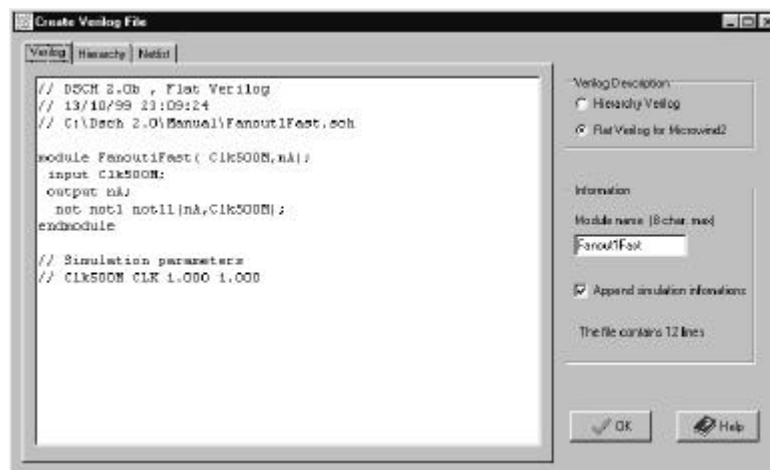
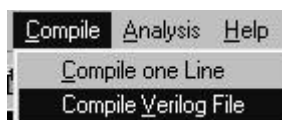


Fig.3.9 Generate a Verilog description of the Inverter

The layout tool Microwind2 is able to translate the Verilog description of the circuit “Inverter” directly into layout. The step-by-step procedure is described below.



① Click on the icon above to activate the Microwind2 software.



② Click *Compile* → *Compile Verilog File* in the main menu. Select “Inverter.TXT” in the list.



③ Click *Compile*. After a few seconds, the layout of the ‘Inverter’ circuit appears, as shown in the figure below.

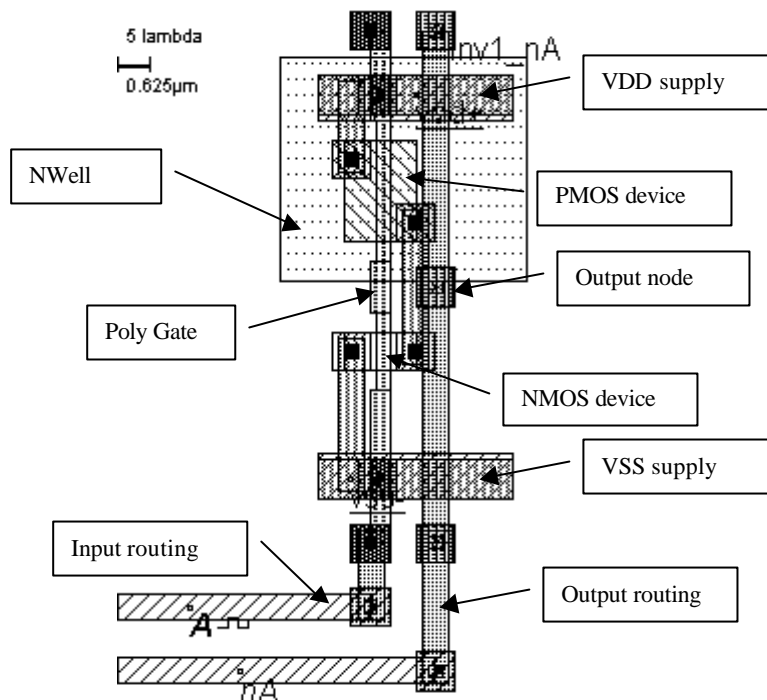


Fig.3.10: The circuit 'Inverter' compiled into layout

5. SIMULATION OF THE INVERTER



④ Click *Simulate* → *Start Simulation* or the icon above. The simulation of the circuit is performed. You may verify the correct behavior of the inverter cell.

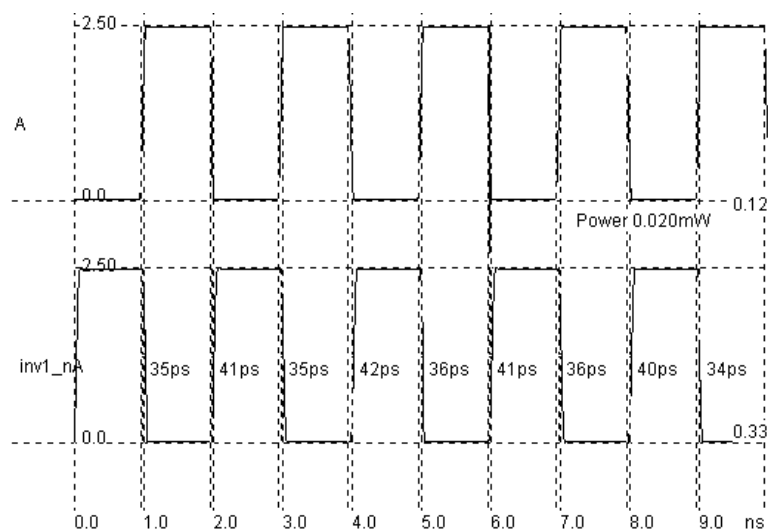


Fig.3.11: The analog simulation of the circuit 'Inverter.MSK' using Microwind2

When comparing logic simulation and analog simulation, some comments may rise:

- The predicted delays are similar (roughly 0.05ns in both cases).
- The predicted power consumption at analog level (3.11) is smaller than at logic level (Fig. 3.7). The explanation is that at logic level, we considered a typical interconnect that acts as a significant capacitance load, thus increasing the power consumption. At analog level, the physical interconnect in the layout of figure 3.10 is a small interconnect, representing a small parasitic load for the inverter, thus reducing the power consumption.

6. VIEWS OF THE PROCESS



**View the Process
in 2D**

The *Process Simulator* shows the vertical aspect of the layout, as when fabrication has been completed. This feature is a significant aid to understand the fabrication principles. A click of the mouse at the first point and the release of the mouse at the second point give the cross section.

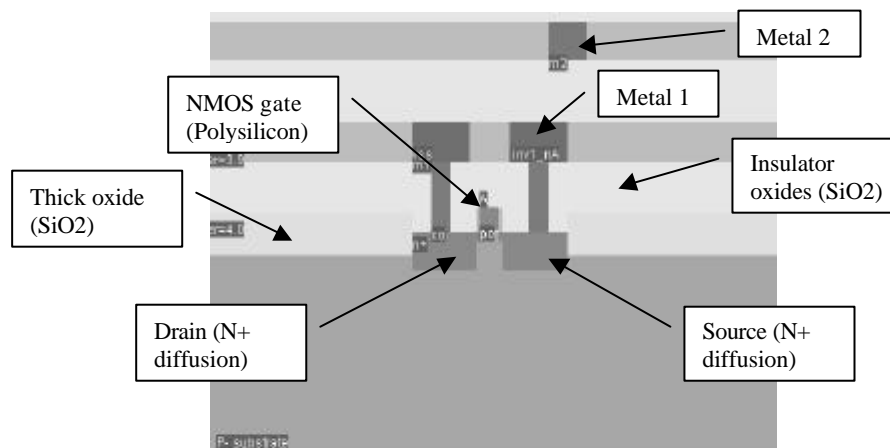


Fig.3.12 The 2D process section of the 'Inverter' circuit near the nMOS device



**Simulate the
Process steps in 3D**

Click *Simulate* → *Process steps in 3D* or the icon above. The simulation of the CMOS fabrication process is performed, step by step. On figure 3.13, the picture on the left represents the nMOS device, pMOS device, common polysilicon gate and contacts. The picture on the right side represents the same portion of layout with the metal layers stacked on the top of the active devices.

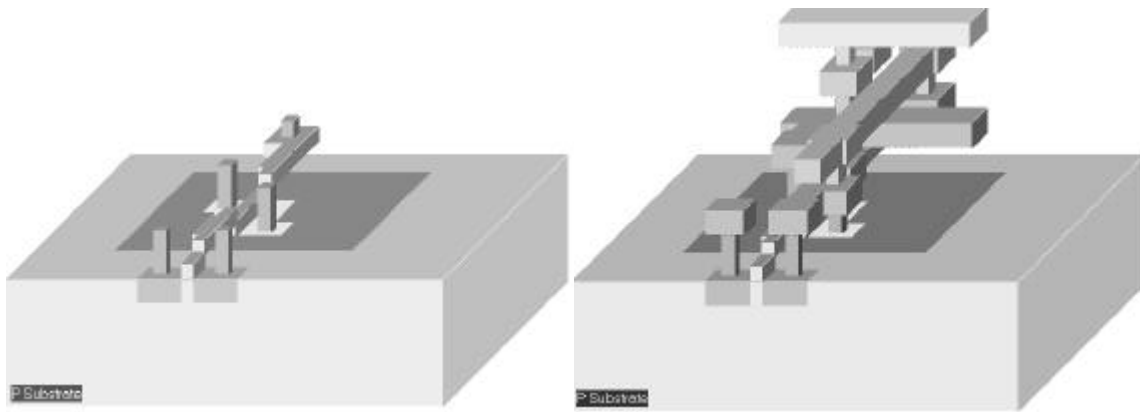


Fig.3.13 The step-by-step fabrication of the 'Inverter' circuit

7. BUFFER

INVERTER	
BUFFER	

A buffer is a set of two chained inverters, used to propagate the logic signal in long wires without altering too severely the delay. The basic idea is to design the second inverter using MOS devices with large width and minimum length. The width is usually 4 to 16 times the basic MOS width. This type of inverter switches rapidly, even if it drives long interconnects and multiple input gates. The buffer is widely used in microelectronics designs. The clock signals, bus, ports and long wires with severe time constraints use such circuits. The main drawback of the strong buffer circuit is the significant power consumption and the consequence of the sharp consumption peak on the global noise when a simultaneous switching occurs.

<Etienne: detail the buffer (inv+big inv, after inv description), and 3-state inverter>

<Etienne: demonstrate the use of a buffer at logic level if you have a smaller delay vs. The load for buffer>

<Etienne: amplifier>

<Illustrate by a long interconnect>

8. 3-STATE INVERTER

INVERTER	
3-STATE INVERTER	

<Etienne: improve>.

Until now all the symbols produced the value logic '0' and logic '1'. However, if two outputs are connected together, as the left circuit shown below, it will provoke a circuit error. In order to avoid such conflicts, specific symbols are used, featuring the possibility to remain in a 'high impedance' state.

The 3-state symbol used below is *Bufif1*, and it consists of the logic buffer and an enable control. There also exists a 3-state inverter *Notif1*. The output remains in 'high impedance' as long as the enable 'En' is set to level '0'. The truth tables are reported below.

NOTIF1		
In	En	Out
x	0	H
0	1	1
1	1	0

Fig. xxx : Wrong (left) and correct (right) way to connect two gates on the same bus

<Also exists Buf if 1>

<Etienne: can I compile 'Bufif1'?>

9. ANALOG BEHAVIOR OF THE INVERTER

<Etienne: inv with various Vc>

10. CONCLUSION

The inverter has been presented in this chapter.

REFERENCES

[1] xxxx

[2] yyy