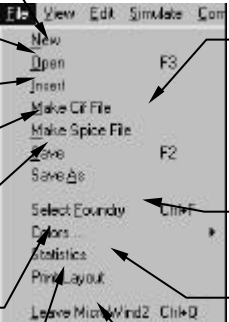
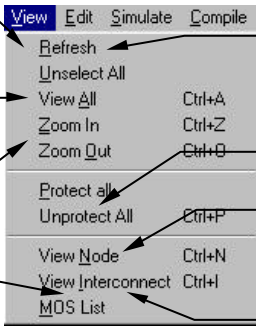
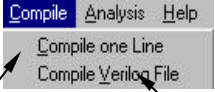
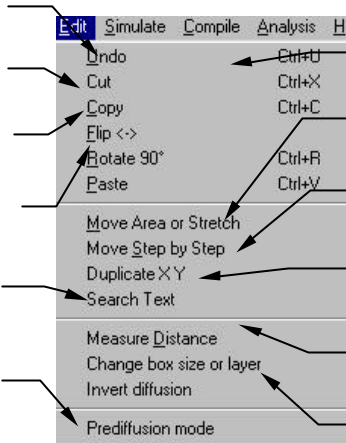
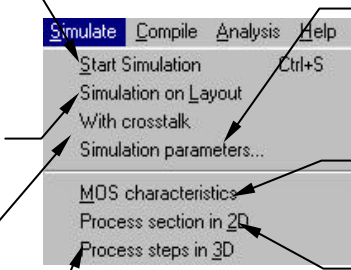
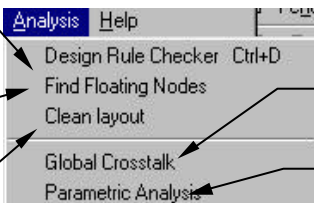
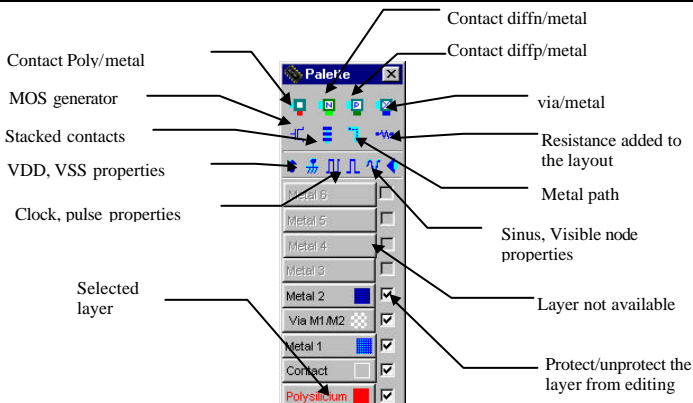


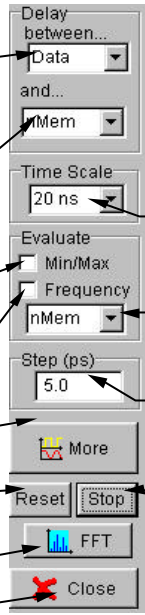
C

Quick
Reference
Sheet




















1. Microwind2 Menus

FILE MENU	 <p>Reset the program and starts with a clean screen</p> <p>Read a layout data file</p> <p>Insert a layout in the current layout</p> <p>Translates the layout into CIF</p> <p>Save the layout</p> <p>Switch to monochrome/Color mode</p> <p>Print the layout</p> <p>Extract the electrical circuit and translates into SPICE</p> <p>Configure Microwind2 to a foundry</p> <p>Layout properties : number of box, devices, size</p> <p>Quit Microwind2 and returns to Windows</p>
VIEW MENU	 <p>Unselect all layers and redraw the layout</p> <p>Fit the window with all the edited layout</p> <p>Zoom In, Zoom out the layout window</p> <p>Give the list of nMOS and pMOS devices</p> <p>Redraw the screen</p> <p>Protect all layers from modifications</p> <p>Extract the electrical node starting at the cursor location</p> <p>Extract the node propagating on metal interconnects</p>
COMPILE MENU	 <p>Compile one single line (on-line)</p> <p>Compile a Verilog file generated by DSCH2</p>

EDIT MENU	<p>Cancel last editing command</p> <p>Cut elements included in an area</p> <p>Duplicate elements included in an area</p> <p>Flip or rotate elements included in an area</p> <p>Search a text label in the label list</p> <p>In prediffusion mode, only metal layers can be edited</p> 
SIMULATE MENU	<p>Extract the electrical circuit and run the simulation</p> <p>Simulate directly on the layout, with a palette of colors representing voltage</p> <p>Include crosstalk effects in simulation</p> <p>View the process steps of the layout fabrication in 3D</p> 
ANALYSIS MENU	<p>Verifies the layout and highlight the design rule violations</p> <p>Gives the list of nodes not connected to diffusion layers</p> <p>Remove redundant or overlapping boxes</p> 
PALETTE	

SIMULATOR WINDOW	<div> <p>Select the node from which the delay counter is started at each crossing of VDD/2</p> <p>The delay counter is stopped at each crossing of VDD/2 and the delay is drawn</p> <p>The minimum and maximum voltage of the selected node are displayed.</p> <p>At each period of the selected node, the frequency is displayed</p> <p>More simulation</p> <p>Restart simulation from time 0</p> <p>Show the FFT of the selected signal</p> <p>Back to the editor</p> </div> <div>  <p>Delay between... Data</p> <p>and... Mem</p> <p>Time Scale 20 ns</p> <p>Evaluate Min/Max</p> <p>Frequency nMem</p> <p>Step (ps) 5.0</p> <p>More</p> <p>Reset</p> <p>Stop</p> <p>FFT</p> <p>Close</p> </div> <div> <p>Select the time scale within a list in the menu</p> <p>Node selected for min/max, freq and FFT calculation</p> <p>Set the time interval between two simulation steps.</p> <p>Stop simulation.</p> </div>
-------------------------	---

LIST OF ICONS

	Open a layout file MSK		Extract and view the electrical node pointed by the cursor
	Save the layout file in MSK format		Extract and simulate the circuit
	Draw a box using the selected layer of the palette		Measure the distance in lambda and micron between two points
	Delete boxes or text.		2D vertical aspect of the device
	Copy boxes or text		Step by step fabrication of the layout in 3D
	Stretch or move elements		Design rule checking of the circuit. Errors are notified in the layout
	Zoom In		Add a text to the layout. The text may include simulation properties.
	Zoom Out		Chip library of contacts, MOS, metal path, 2-metal routing, pads, etc...
	View all the drawing		Static MOS characteristics
			View the palette

2. Dsch2 Menus

<To be completed>

3. List of Files

FILE	DESCRIPTION
MICROWIND2.EXE	Main software
MICROWIND2.HLP	Help manual
*.ppt	PowerPoint © Slides illustrating the technology scale down, models, design and signal integrity
*.RUL	TECHNOLOGY FILES. The MICROWIND2 program reads the rule file to update the simulator parameters, the design rules and parasitic capacitor values. A detailed description of the .RUL file is reported at the end of Appendix A.
*.MSK	LAYOUT FILES. The MICROWIND2 software creates data files with the appendix .MSK Those files are simple text files containing the list of boxes and layers, and the list of text declarations.
*.CIR	The command File -> Make SPICE File generates a SPICE compatible text description.
*.MES	MOS I/V Measurements
*.TXT	Verilog text inputs

4. List of Measurement Files

In the package, a selection of measurements are proposed, for comparison between real case measurements and models. Four chips have been fabricated and measured in our laboratory:

- Chip « a » (0.35µm ST)
- Chip « b » (0.25µm ST)
- Chip « c » (0.18µm ST)
- Chip "d" (0.8µm ATMEL-ES2)

Measurement files	Description
0.35µm CMOS Na10x0,4.mes Na10x10.mes Na10x2.mes Na1x0,4.mes Na80x0,4.mes Pa10x0,4.mes Pa10x10.mes Pa10x2.mes Pa1x0,4.mes Pa80x0,4.mes	Nmos W=10µm, L=0.4µm (0.35 effective) Nmos W=10µm, L= 10µm Nmos W=10µm, L= 2µm Nmos W=1µm, L= 0.4µm Nmos W=80µm, L= 0.4µm Pmos W=10µm, L= 0.4µm Pmos W=10µm, L= 10µm Pmos W=10µm, L= 2µm Pmos W=1µm, L= 0.4µm Pmos W=80µm, L= 0.4µm
0.25µm CMOS Nb10x0,25.mes Nb10x10.mes	Nmos W=10µm, L=0.25µm Nmos W=10µm, L=10µm
0.18µm CMOS Nc10x10.mes NcHS4x0.2.mes NcHV4x0.2.mes Nc4x0.2.mes	Nmos W=10µm, L=10µm Nmos W=4µm, L=0.2µm high speed option Nmos W=4µm, L=0.2µm high voltage option Nmos W=4µm, L=0.2µm normal (low leakage)

0.8µm CMOS Nd20x20.mes Nd20x0,8.mes	Nmos W=20µm, L=20µm Nmos W=20µm, L=0.8µm
---	---

Measurement file example

```

Measure v3.0 - 4 May 00
LL 10x10um cmos018
NMOS 10.0 10.0
IDVd 5 0.0 2.0 0.5
41 0
0.0 0.0 0.0 0.0 0.0 0.0
5.0000E-02 2.0226E-12 6.7235E-07 6.4727E-06 1.1584E-05 1.5635E-05
1.0000E-01 2.3586E-12 7.7469E-07 1.2143E-05 2.2459E-05 3.0636E-05
1.5000E-01 2.4540E-12 7.8616E-07 1.7012E-05 3.2623E-05 4.5003E-05
2.0000E-01 2.5151E-12 7.8892E-07 2.1089E-05 4.2079E-05 5.8736E-05
2.5000E-01 2.5716E-12 7.9037E-07 2.4386E-05 5.0826E-05 7.1835E-05
3.0000E-01 2.6275E-12 7.9158E-07 2.6929E-05 5.8867E-05 8.4301E-05
3.5000E-01 2.6834E-12 7.9273E-07 2.8768E-05 6.6202E-05 9.6133E-05
4.0000E-01 2.7393E-12 7.9387E-07 2.9992E-05 7.2834E-05 1.0733E-04
...
2.0000E+00 4.5477E-12 8.3166E-07 3.2021E-05 1.0562E-04 2.0746E-04
IdVg 4 0.0 -1.5 -0.5 0.05
21 0
0.0 2.0226E-12 5.7123E-13 1.0630E-12 1.5644E-12
1.0000E-01 3.4083E-11 7.6465E-13 1.0653E-12 1.5644E-12
2.0000E-01 5.7669E-10 4.6877E-12 1.1181E-12 1.5655E-12
3.0000E-01 8.9864E-09 8.3526E-11 2.2992E-12 1.5922E-12
...
1.9000E+00 1.4895E-05 1.3132E-05 1.1692E-05 1.0455E-05
2.0000E+00 1.5635E-05 1.3899E-05 1.2479E-05 1.1259E-05

```


5. *Instructor's Guide*






POWERPOINT SLIDES (4H)

A set of PowerPoint 97™ slides is given in the CD-ROM, based on the extensive use of DSCH2 and MICROWIND2 to introduce microelectronics in a clear and attractive way.

Slides_Technology.ppt	Illustration of the technology scale down
Slides_Models.ppt	An overview of MOS, interconnect, IO and package models
Slides_Design.ppt	Illustration of main design techniques
Slides_Integrity.ppt	Introduction to signal integrity

TUTORIAL ON MOS (2H)

The Microwind2 program may be used for a beginning electronics class to design a single MOS, to add clocks and see how the MOS device is turned on or off. Conduct a step by step manual design of the MOS, which provides the student with a good introduction to the basic commands.

	Draw the device layers (n+ diffusion, poly,)
	Add contacts to Gate, Drain and Source
	Look at the cross-section of the transistor
	Look at the I/V characteristics of your device
	Simulate the MOS and verify the switch function

Possible questions to ask students include the following:

- Give an approximation of the threshold voltage. It should be 0.5-0.7V.
- Find the maximum current I_{ds} available. It should be the order of 1mA.
- Modify the width ($4\lambda \rightarrow 8\lambda$) and find the new I_{ds} maximum. It should be twice as wide as the previous one, because of the law $I_{ds}=W/L$.
- Modify the temperature (**Simulate->Simulate Options**). It is not obvious that a lower temperature makes the device run faster. Many students tend to think the opposite way.
- Switch to the simulation of the p-channel MOS. Point out the problem of the reduced mobility ($\mu_n=500 \text{ cm}^2/\text{V.s}$, $\mu_p=250 \text{ cm}^2/\text{V.s}$)

DESIGN OF CMOS CELLS (16H)

It will take about 16 hours to cover the design and simulations of an inverter, a logic gate, a complex gate, an arithmetic circuit, an amplifier and a converter. This program allows students to design and simulate an IC.

Although a very user-friendly and highly intuitive program, students should nevertheless learn its basis with an instructor. Three-four hour sessions should be sufficient to learn about this package and use it. We recommend the following procedure:

- Conduct a step by step manual design of the inverter as shown in Chapter 3. This provides the student with a good introduction to the basic commands
- Simulate your inverter. Minor problems may occur if the VDD and VSS buses are not correctly polarized. Make a ring-oscillator and observe the resulting frequency.
- Change the design rules from 0.8 μ m 2-metal technology (cmos08.rul) to advanced sub-micron technology (cmos012.rul) and see the effects of oscillating frequency.
- Use the DSCH2 logic editor to design a schematic diagram, for example a half adder. Verify its logic behavior. Click on « **Make Verilog File** » and save the file. Then compile the VERILOG text file using the Microwind2 command « **Compile Verilog File** ». Verify the correct analog behavior of the cell.
- Conduct arithmetic, latch or analog cell projects or projects such as: Schmitt Trigger, Multiplier, Follower, Shift register, RAM design, converter design or PLL design.